Safe Harbor for Forward-Looking Statements; Other Disclosures

This presentation contains forward-looking statements under the Private Securities Litigation Reform Act of 1995, including those relating to Rambus’ expectations regarding business opportunities, the Company’s ability to deliver long-term, profitable growth, industry growth rates, the successful integration of AnalogX and PLDA, product and investment strategies, the long-term sustainability of the Company’s increased product revenue and cash generated from operating activities, the Company’s outlook and financial guidance for the first quarter of 2022 and related drivers, and the Company’s ability to effectively manage supply chain shortages.

Such forward-looking statements are based on current expectations, estimates and projections, management’s beliefs and certain assumptions made by the Company’s management. Actual results may differ materially. The Company’s business generally is subject to a number of risks which are described more fully in Rambus’ periodic reports filed with the Securities and Exchange Commission, as well as the potential adverse impacts related to, or arising from, the Novel Coronavirus (COVID-19) and its variants. The Company undertakes no obligation to update forward-looking statements to reflect events or circumstances after the date hereof.

Effective January 1, 2018, the Company adopted Accounting Standards Update No. 2014-09, Revenue from Contracts with Customers in ASC 606. The adoption of ASC 606 materially impacted the timing of revenue recognition for the Company's fixed-fee intellectual property licensing arrangements. The adoption of ASC 606 did not have a material impact on the Company’s other revenue streams, net cash provided by operating activities, or its underlying financial position.

This presentation contains non-GAAP financial measures, including operating costs and expenses, interest and other income (expense), net and diluted net income (loss) per share. In computing these non-GAAP financial measures, stock-based compensation expenses, acquisition-related transaction costs and retention bonus expense, amortization expenses, depreciation expense on unused Electronic Design Automation ("EDA") software licenses, expense on abandoned operating leases, restatement and shareholder activist costs, facility restoration costs, non-cash interest expense and certain other one-time adjustments were considered. The non-GAAP financial measures should not be considered a substitute for, or superior to, financial measures calculated in accordance with GAAP, and the financial results calculated in accordance with GAAP and reconciliations from these results should be carefully evaluated. Management believes the non-GAAP financial measures are appropriate for both its own assessment of, and to show investors, how the Company’s performance compares to other periods. Reconciliation from GAAP to non-GAAP results are made available and more fully described on our website as well as the back of this deck and in the earnings release.
Rambus at a Glance

Pioneer of industry-leading chips and silicon IP making data faster and safer

- Improving data bandwidth, capacity and security
- 30+ Years Tech leadership & innovation
- YoY Revenue Growth from Products, Contract and Other* ▲18%
  *Excludes discontinued businesses
- HQ in California with offices WW in India, EU and Asia ~700 Employees Worldwide
- Strong balance sheet and cash generation fuel strategic initiatives 2021 $209M Cash from Operations
- Continued Innovation feeds licensing and product roadmap ~3000 Patents and Applications
- Share of product* revenue from Data Center & Edge 75%+
  *Includes Product and Contract & Other
- Data Center revenue from Data Center & Edge 75%+

~3000 Patents and Applications

Employees Worldwide

HQ in California with offices WW in India, EU and Asia

30+ Years Tech leadership & innovation

YoY Revenue Growth from Products, Contract and Other* ▲18%
  *Excludes discontinued businesses

Strong balance sheet and cash generation fuel strategic initiatives 2021 $209M Cash from Operations

Continued Innovation feeds licensing and product roadmap ~3000 Patents and Applications

Share of product* revenue from Data Center & Edge 75%+
  *Includes Product and Contract & Other
MORE AND MORE DATA
Data usage growing at 35% CAGR to 175ZB by 2025, driving overall server unit growth up 8% per year

ACCELERATING SHIFT TO CLOUD
Cloud driving Data Center growth, with equipment spend at top 5 hyperscalers doubling to $100B by 2024

GROWING AI/ML ADOPTION
Over 25% of server shipments in 2025 will be AI-specific with $10B in AI silicon

PROCESSING AT THE EDGE
Edge workloads increasing by 34% per year leading to $5B in Edge silicon by 2024

SECURITY THREATS ON THE RISE
Total number of DDoS attacks projected to double from 7.9M in 2018 to 15.4M in 2023

INCREASING CONNECTIVITY
In 2021, there were 27B connected smart devices capturing and sending data, up 10B over 5 years

HARDWARE SECURITY IS MISSION CRITICAL TO PROTECT VALUABLE DATA

MEMORY AND I/O BANDWIDTH LIMITING FACTOR FOR SYSTEM PERFORMANCE

RAPID DATA CENTER GROWTH DRIVING TECHNOLOGY DEMAND
Amplified Market Opportunity
Increasing need for bandwidth and security

**FORECASTED ANNUAL GROWTH**

- **Market**: ↑4.5%: Data Center
  - Exponential rise in data usage driving secular growth
- **System**: ↑8%: Server Units
  - Rising AI/ML workloads driving server growth
- **Chip**: ↑26%: Server DRAM Bits
  - Need for more data driving memory bandwidth and bit growth

*Source: Arizton, IDC, Gartner*
Semiconductor Industry Ecosystem Built on Leading-Edge IP

Markets
Data Center
5G/Edge
IoT
Automotive
Government

Cloud Providers
Google
amazon
facebook
Microsoft
Alibaba Group

System OEMs
hp
dell
Quanta Computer
BOSCH
ERICSSON

Platform and Module
SK hynix
SAMSUNG
Micron
Qualcomm
AMD
intel

Chip Makers
Rambus
RENESAS
MONTAGE Technology
MICROCHIP

Foundry
tsmc
SAMSUNG
GLOBAL FOUNDRIES
intel

Technology Suppliers
Rambus
cadence
SYNOPSYS
arm

Ecosystem Example
Rambus Memory Interface Chip Growth

2018-2021

55% CAGR
Rambus Product Revenue (~Chips)

• Robust server memory demand projected through 2023
• Enhanced qualification footprint on new DDR4 platforms
• Strong market position on DDR5 platforms, shipping Gen1 RCD in volume
• First to sample Gen2 RCD at industry’s fastest data rate of 5600 MT/s
New Memory Architectures Driving TAM Expansion

Transition to DDR5

Memory Subsystem Expansion with Serial Links (e.g., CXL)

Data Center Disaggregation

Increasing bandwidth, capacity, efficiency and security
CXL Interconnect Initiative

- Establishes focused development effort on breakthrough solutions for memory expansion and pooling for advanced data center architectures
- Complements existing memory interface chip business and leverages in-house expertise in high-speed I/O, memory and security

Expansion provides more main memory to Host (CPU) for higher performance on high-capacity workloads

Pooling provides additional main memory to Hosts on an “as needed” basis, improving performance, efficiency and TCO. Pooling ultimately supports disaggregation and composability.
Rambus Delivers Fast and Secure Connections for Data Center

Memory and SerDes IP: Accelerate data for AI
Memory Interface Chips: Improve memory subsystem speed and capacity
Secure Silicon IP: Protect valuable data

Faster Data Rates
Greater Capacity
Higher Security
Easy Integration
Reliable Supplier
Product Leadership Driving Topline Growth

2018-2021

39% CAGR
Chip and Silicon IP* combined revenue

Industry’s first and fastest DDR5 memory interface chips

Integrated PCIe5, CXL 2.0, HBM3/2E and GDDR6 PHY + Controller subsystems

Broadest portfolio of secure root of trust, protocol engine, and crypto accelerator cores

Experts in interconnect solutions critical for performance and utilization in emerging data center architectures

*Product and Contract and Other combined revenue
**Financial Highlights**

**Chip & Silicon IP Revenue* ($M)**

- **2019**: 115, Discontinued Business: 19
- **2020**: 162
- **2021**: 192

**Pro Forma Operating Expenses ($M)**

- **2019**
  - R&D: 80
  - SG&A: 144
  - Total: 224
- **2020**
  - R&D: 69
  - SG&A: 123
  - Total: 192
- **2021**
  - R&D: 68
  - SG&A: 120
  - Total: 189

**Cash from Operations ($M) & FCF per Share ($)**

- **2019**: Cash from Ops: 129, FCF per Share: 1.02
- **2020**: Cash from Ops: 185, FCF per Share: 1.26
- **2021**: Cash from Ops: 209, FCF per Share: 1.66

**Cash Equivalents & Return of Capital ($M)**

- **2019**: Cash Equivalents: 408, Return of Capital: 67
- **2020**: Cash Equivalents: 503, Return of Capital: 50
- **2021**: Cash Equivalents: 486, Return of Capital: 97

*Includes Product and Contract & Other Revenue*
Rambus Investment Summary

- Amplified data center market opportunity as memory relevance continues to grow
- Pioneer of industry-leading chips and silicon IP enabling critical performance improvements for data center and cloud
- Continued innovation feeds patent portfolio and product roadmap expansion
- Focus on strategic initiatives drives financial results and profitable growth
- Strong cash generation enables strategic initiatives and return of capital to shareholders
Detailed Financials
## Outstanding Cash Generation

<table>
<thead>
<tr>
<th>In Millions</th>
<th>ASC 606 Q4 2020</th>
<th>ASC 606 Q1 2021</th>
<th>ASC 606 Q2 2021</th>
<th>ASC 606 Q3 2021</th>
<th>ASC 606 Q4 2021</th>
</tr>
</thead>
<tbody>
<tr>
<td>Revenue</td>
<td>$61.9</td>
<td>$70.4</td>
<td>$84.9</td>
<td>$81.3</td>
<td>$91.8</td>
</tr>
<tr>
<td>Total Operating Costs and Expenses¹</td>
<td>$55.8</td>
<td>$58.2</td>
<td>$56.1</td>
<td>$62.8</td>
<td>$65.4</td>
</tr>
<tr>
<td>Operating Income¹</td>
<td>$6.1</td>
<td>$12.1</td>
<td>$28.8</td>
<td>$18.5</td>
<td>$26.4</td>
</tr>
<tr>
<td>Cash from Operations</td>
<td>$42.1</td>
<td>$39.5</td>
<td>$51.6</td>
<td>$46.0</td>
<td>$72.2</td>
</tr>
</tbody>
</table>

- Revenue: Driven by higher product revenue quarter over quarter
- Total Operating Costs and Expenses: Disciplined R&D investment to support strategic growth initiatives
- Operating Income: Operating results under ASC 606 do not reflect significant cash flows from fixed-fee licensing arrangements
- Cash from Operations: Outstanding cash generation

¹Please refer to reconciliations of non-GAAP financial measures included in this presentation and in our earnings release
## Strong Balance Sheet Supports Strategic Initiatives

<table>
<thead>
<tr>
<th></th>
<th>Q4 2020</th>
<th>Q1 2021</th>
<th>Q2 2021</th>
<th>Q3 2021</th>
<th>Q4 2021</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Total Cash &amp; Marketable Securities</strong></td>
<td>$502.6</td>
<td>$529.1</td>
<td>$477.1</td>
<td>$419.7</td>
<td>$485.6</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Total Assets</strong></td>
<td>$1,251.4</td>
<td>$1,235.8</td>
<td>$1,153.0</td>
<td>$1,202.7</td>
<td>$1,232.6</td>
</tr>
<tr>
<td><strong>Stockholders’ Equity</strong></td>
<td>$912.7</td>
<td>$909.4</td>
<td>$830.6</td>
<td>$847.8</td>
<td>$862.4</td>
</tr>
<tr>
<td><strong>Cash from Operations</strong></td>
<td>$42.1</td>
<td>$39.5</td>
<td>$51.6</td>
<td>$46.0</td>
<td>$72.2</td>
</tr>
</tbody>
</table>
## Reconciliation of Non-GAAP Financial Measures

### Net Income (Loss) in Millions

<table>
<thead>
<tr>
<th></th>
<th>Q4 2020 (ASC 606)</th>
<th>Q1 2021 (ASC 606)</th>
<th>Q2 2021 (ASC 606)</th>
<th>Q3 2021 (ASC 606)</th>
<th>Q4 2021 (ASC 606)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GAAP Net Income (Loss)</td>
<td>($12)</td>
<td>($3)</td>
<td>$11</td>
<td>$4</td>
<td>$6</td>
</tr>
<tr>
<td><strong>Adjustments:</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Stock-based compensation</td>
<td>$6</td>
<td>$7</td>
<td>$7</td>
<td>$7</td>
<td>$6</td>
</tr>
<tr>
<td>Acquisition-related costs and retention bonus expense</td>
<td>$1</td>
<td>$1</td>
<td>$2</td>
<td>$2</td>
<td>$1</td>
</tr>
<tr>
<td>Amortization of acquired intangible assets</td>
<td>$5</td>
<td>$5</td>
<td>$5</td>
<td>$4</td>
<td>$4</td>
</tr>
<tr>
<td>Restructuring and other charges</td>
<td>$3</td>
<td>$0</td>
<td>$0</td>
<td>$0</td>
<td>$0</td>
</tr>
<tr>
<td>Non-cash interest expense</td>
<td>$2</td>
<td>$2</td>
<td>$2</td>
<td>$2</td>
<td>$2</td>
</tr>
<tr>
<td>Facility restoration costs</td>
<td>$0</td>
<td>$0</td>
<td>$0</td>
<td>$0</td>
<td>$0</td>
</tr>
<tr>
<td>Depreciation expense on unused EDA software licenses</td>
<td>$2</td>
<td>$0</td>
<td>$0</td>
<td>$0</td>
<td>$0</td>
</tr>
<tr>
<td>Expense on abandoned operating leases</td>
<td>$0</td>
<td>$1</td>
<td>$1</td>
<td>$1</td>
<td>$1</td>
</tr>
<tr>
<td>Restatement and shareholder activist costs</td>
<td>$0</td>
<td>$3</td>
<td>$0</td>
<td>$0</td>
<td>$0</td>
</tr>
<tr>
<td>Provision for (benefit from) income taxes</td>
<td>($0)</td>
<td>($4)</td>
<td>($5)</td>
<td>($4)</td>
<td>($5)</td>
</tr>
<tr>
<td>Change in fair value of earn-out liability</td>
<td>$0</td>
<td>$0</td>
<td>$0</td>
<td>$0</td>
<td>$5</td>
</tr>
<tr>
<td>Non-GAAP Net Income</td>
<td>$6</td>
<td>$11</td>
<td>$23</td>
<td>$16</td>
<td>$21</td>
</tr>
</tbody>
</table>

### Operating Income (Loss) in Millions

<table>
<thead>
<tr>
<th></th>
<th>Q4 2020 (ASC 606)</th>
<th>Q1 2021 (ASC 606)</th>
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<th>Q3 2021 (ASC 606)</th>
<th>Q4 2021 (ASC 606)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GAAP Operating Income (Loss)</td>
<td>($11)</td>
<td>($3)</td>
<td>$14</td>
<td>$5</td>
<td>$9</td>
</tr>
<tr>
<td><strong>Adjustments:</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Stock-based compensation</td>
<td>$6</td>
<td>$7</td>
<td>$7</td>
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<td>$6</td>
</tr>
<tr>
<td>Acquisition-related costs and retention bonus expense</td>
<td>$1</td>
<td>$1</td>
<td>$2</td>
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<td>$1</td>
</tr>
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<td>$5</td>
<td>$5</td>
<td>$4</td>
<td>$4</td>
</tr>
<tr>
<td>Restructuring and other charges</td>
<td>$3</td>
<td>$0</td>
<td>$0</td>
<td>$0</td>
<td>$0</td>
</tr>
<tr>
<td>Facility restoration costs</td>
<td>$0</td>
<td>$0</td>
<td>$0</td>
<td>$0</td>
<td>$0</td>
</tr>
<tr>
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<td>$0</td>
<td>$0</td>
<td>$0</td>
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<tr>
<td>Expense on abandoned operating leases</td>
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<td>$1</td>
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<td>$3</td>
<td>$0</td>
<td>$0</td>
<td>$0</td>
</tr>
<tr>
<td>Change in fair value of earn-out liability</td>
<td>$0</td>
<td>$0</td>
<td>$0</td>
<td>$0</td>
<td>$5</td>
</tr>
<tr>
<td>Non-GAAP Operating Income</td>
<td>$6</td>
<td>$12</td>
<td>$29</td>
<td>$19</td>
<td>$26</td>
</tr>
</tbody>
</table>

- Depreciation: $7 | $5 | $5 | $5 | $6 |
- Adjusted EBITDA: $13 | $17 | $34 | $24 | $32 |

Certain amounts may be off $1.0M due to rounding.
# Revenue and Licensing Billings

<table>
<thead>
<tr>
<th>In Thousands</th>
<th>ASC 606</th>
<th>ASC 606</th>
</tr>
</thead>
<tbody>
<tr>
<td>Royalty Revenue</td>
<td>$21,482</td>
<td>$18,744</td>
</tr>
<tr>
<td>Product Revenue</td>
<td>$30,728</td>
<td>$31,725</td>
</tr>
<tr>
<td>Contract and Other Revenue</td>
<td>$13,567</td>
<td>$11,248</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>$65,777</strong></td>
<td><strong>$61,717</strong></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>In Thousands</th>
<th>ASC 606</th>
<th>ASC 606</th>
</tr>
</thead>
<tbody>
<tr>
<td>Royalty Revenue</td>
<td>$21,482</td>
<td>$18,744</td>
</tr>
<tr>
<td>Licensing Billings¹</td>
<td>$67,072</td>
<td>$60,687</td>
</tr>
<tr>
<td><strong>Delta</strong></td>
<td><strong>$45,590</strong></td>
<td><strong>$41,943</strong></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>In Thousands</th>
<th>ASC 606</th>
<th>ASC 606</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASC 606 Interest Income²</td>
<td>$4,437</td>
<td>$3,788</td>
</tr>
</tbody>
</table>

¹ Licensing billings is an operational metric that reflects amounts invoiced to our patent and technology licensing customers during the period, as adjusted for certain differences.

² Interest income associated with the significant financing component of licensing agreements as a result of the adoption of ASC 606.
## GAAP to Non-GAAP Income Statement

<table>
<thead>
<tr>
<th>In $ Millions</th>
<th>GAAP Actual Q4’21</th>
<th>Non-GAAP Actual Q4’21</th>
<th>Delta to GAAP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Revenue</td>
<td>$91.8</td>
<td>$91.8</td>
<td>$-</td>
</tr>
<tr>
<td>Cost of revenue</td>
<td>17.7</td>
<td>14.0</td>
<td>(3.7)</td>
</tr>
<tr>
<td>Research and development</td>
<td>36.3</td>
<td>32.0</td>
<td>(4.2)</td>
</tr>
<tr>
<td>Sales, general and administrative</td>
<td>23.5</td>
<td>19.4</td>
<td>(4.2)</td>
</tr>
<tr>
<td>Change in fair value of earn-out liability</td>
<td>5.3</td>
<td>0.0</td>
<td>(5.3)</td>
</tr>
<tr>
<td>Total operating cost and expenses</td>
<td>82.8</td>
<td>65.4</td>
<td>(17.4)</td>
</tr>
<tr>
<td>Operating income</td>
<td>9.0</td>
<td>26.4</td>
<td>17.4</td>
</tr>
<tr>
<td>Interest and other income (expense), net</td>
<td>(1.1)</td>
<td>0.8</td>
<td>2.0</td>
</tr>
<tr>
<td>Income before income taxes</td>
<td>7.9</td>
<td>27.2</td>
<td>19.3</td>
</tr>
<tr>
<td>Provision for income taxes</td>
<td>1.8</td>
<td>6.5</td>
<td>4.8</td>
</tr>
<tr>
<td>Net income</td>
<td>$6.1</td>
<td>$20.7</td>
<td>$14.6</td>
</tr>
</tbody>
</table>

Certain amounts may be off $0.1M due to rounding.
Product Overview
Semiconductor Solutions Built on Leading-Edge IP

- **Architecture License**
  - Foundational IP

- **Silicon IP**
  - Security IP: Secure Cores and Provisioning
  - Interface IP: Memory and SerDes PHYs and Controllers

- **Chips**
  - Memory Interface Chips

21
Innovating to Meet Market Needs

Growing Patent Portfolio

- Fundamental R&D feeds product development
- Relevant portfolio regularly cited by major industry players
- Supports predictable licensing base and sustained cash generation

Industry Recognition of Rambus Patents

Source: Innography, patent citations
Memory Interface Chips
Built for speed, power efficiency and reliability, the DDRn memory interface chips for RDIMM, LRDIMM and NVDIMM server modules deliver top-of-the-line performance and the capacity needed to meet the growing demands on enterprise and data center systems.

**Industry-leading Performance**
- Fully-compliant with the latest JEDEC standards
- Operational speeds up to 5600 MT/s

**Enhanced Margin**
- Wide margin I/O design with advanced programmability
- Exceed JEDEC reliability standards for ESD and EOS

**Optimized Power**
- Advanced power management
- Frequency-based, low-power optimization

**Superior Debug and Serviceability**
- Integrated tools for bring-up and debug
- Works out-of-the-box with no BIOS changes required
Memory Interface Chips

Enabling performance and capacity in server DIMMs

**DDR5**
- RCD & DB
- Per JEDEC Direction
- Speeds of 5600 MT/s
- Ongoing qualifications
- AVAILABLE IN PRODUCTION

**DDR4**
- RCD & DB
- JEDEC Compliant
- Speeds up to 3200 MT/s
- Multiple OEM qualifications
- AVAILABLE IN PRODUCTION

**NV**
- DDR4 NVRCD
- JEDEC Compliant
- Speeds up to 3200 MT/s
- Ongoing qualifications
- AVAILABLE IN PRODUCTION

**DDR3**
- RCD & DB
- JEDEC Compliant
- Speeds up to 2133 MT/s
- Multiple OEM qualifications
- AVAILABLE IN PRODUCTION

Smart tools for easy integration and reduced time to market

LabStation Platform and Buffer BIOS Integration Tool

Validated solutions with partners

Validated solutions with partners
DDR DIMMs Boost Capacity and Bandwidth

DIMM Memory Interface chips reduce the number of loads to enable higher system capacity and performance.

Memory Interface Chips = RCD + DB

DDR5 Registered DIMM (RDIMM)

DDR5 Load Reduced DIMM (LRDIMM)
Silicon IP
Across a broad spectrum of applications spanning automotive, artificial intelligence (AI), Internet of Things (IoT), network edge, and data center, there is a common need to move more data faster. Rambus memory and SerDes IP deliver the performance needed by the most demanding applications to move the data at blinding fast speeds.

**HBMM3/2E Memory Subsystem**
- Fully-integrate and silicon-proven PHY and controller
- Running at industry’s fastest data rate up to 8.4 Gbps
- Ideal for AI/ML training, graphics and networking applications

**GDDR6 Memory Subsystem**
- Fully-integrate and silicon-proven PHY and controller
- Running at industry’s fastest data rate up to 18.0 Gbps
- Ideal for AI/ML interference, automotive, graphics and networking applications

**PCIe 5/CXL 2 Interconnect Subsystem**
- Co-validated PHY and controller
- Incorporates industry-leading zero-latency IDE
- Multiple configurations to support broad range of applications
# Memory Interface Solutions

## Memory PHY and digital controller solutions

<table>
<thead>
<tr>
<th>Technology</th>
<th>Capacity</th>
<th>Technology</th>
<th>Capacity</th>
<th>Technology</th>
<th>Capacity</th>
</tr>
</thead>
<tbody>
<tr>
<td>HBM3</td>
<td>8.4 Gbps</td>
<td>HBM2E</td>
<td>3.6 Gbps</td>
<td>GDDR6</td>
<td>12-18 Gbps</td>
</tr>
<tr>
<td>7 &amp; 11nm</td>
<td></td>
<td>7nm</td>
<td></td>
<td>7nm</td>
<td></td>
</tr>
<tr>
<td>2.5D design architecture</td>
<td></td>
<td>1024-bit</td>
<td></td>
<td>1024-bit</td>
<td></td>
</tr>
<tr>
<td>DDR4/3</td>
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<tr>
<td>12 &amp; 28nm</td>
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<tr>
<td>3200 Mbps</td>
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<tr>
<td>1-4 Ranks</td>
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<tr>
<td>DFI 4.0</td>
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</tbody>
</table>

## Integrated tools for easy bring-up and characterization

- Easy-to-use PC Interface
- Interface to 3rd party software
- Pre-defined test scripts
- PHY control settings
- External instrument control
- System characteristics and analysis

## Verification tools

- 8.4 Gbps
- 1024-bit
- 2.5D design architecture
- 3200 Mbps
- x16 to x72-bits
- 1-4 Ranks
- DFI 4.0

---

*Data • Faster • Safer*
Complete HBM3 Memory Subsystem

Applications
• AI/ML
• Graphics
• Networking

Features
• Industry’s highest data rate: 8.4 Gbps
• 1075.2 GB/s maximum bandwidth
• 16 channels at 64 bits/channel
• Support for stacks up to 16 DRAM

HBM3 Memory Subsystem (Controller & PHY)

2.5D/3D System Architecture with HBM3 Memory
Complete GDDR6 Memory Subsystem

Applications:
• AI/ML
• Automotive
• Graphics
• Networking

Features:
• JEDEC standard compliant
• 7nm process node
• 72 GB/s maximum bandwidth
• Speed Bins: 12, 14, 16, 18 Gbps
• Supported DRAM: 8, 12, 16 Gbit
• ASIC Interface: DFI style
• Supports clam shell mode
• All training and calibration modes support
## High-Speed Interconnect Solutions

### PHY and digital controller solutions

<table>
<thead>
<tr>
<th>PCIe 6 Controller</th>
<th>PCIe 5 CXL 2</th>
<th>32G</th>
<th>28G</th>
</tr>
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<tbody>
<tr>
<td>PCIe 6</td>
<td>PCIe 5</td>
<td>CEI-28/25/11</td>
<td>CEI-28/25/11</td>
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<tr>
<td>PCIe 5/4/3/2</td>
<td>CXL 2/1.1</td>
<td>40/10GbE</td>
<td>40/10GbE</td>
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<td></td>
<td>PCIe 4/3/2</td>
<td>JESD204B/C</td>
<td>FC28</td>
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<td>CPRI</td>
<td>XFI/XAUI</td>
</tr>
</tbody>
</table>

### Integrated tools for easy bring-up and characterization

- Easy-to-use PC Interface
- Interface to 3rd party software
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- PHY control settings
- External instrument control
- System characteristics and analysis

### Verification tools

- LabStation Platform

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Data • Faster • Safer
Complete PCIe 5.0 Interface Subsystem

Co-validated PCIe 5 PHY and Controller
- Eases SoC integration effort
- Reduces design risk
- Speeds time to market

Features
- Backward compatible to PCIe 4/3/2
- PHY supports Compute Express Link (CXL)
- X1, X2, X4, X8, and X16 lane configuration support
- Supports >36dB of channel insertion loss
- Available in 7nm

Rambus PCIe 5.0 Interface Subsystem
PCIe 6.0 Controller with IDE

- PCIe 6.0 compliant Digital Controller core
- 64 GT/s performance
- Integrated IDE with ultra-low latency
- Optimized for power and area
- Builds on track record of 400+ PCIe controller production tape outs
- Leverages industry leadership in security IP
CXL 2.0 Controller with Zero—Latency IDE

- Low latency and high data rates are critical to the memory-cache coherent use cases enabled by CXL

- Integrity and Data Encryption (IDE) monitors and protects against physical attacks on CXL and PCIe links

- A zero latency IDE provides robust data protection with no sacrifice in performance
Rambus secure silicon IP helps protect data at rest and in motion across a broad range of applications and throughout a device’s lifecycle. Securing electronic systems at their hardware foundation, our embedded security solutions span areas including root of trust, tamper resistance, content protection, and trusted provisioning.

**Root of Trust Cores**
- Portfolio of solutions from fully-programmable secure co-processors to highly-compact state machines
- Provides hardware-based foundation for security
- Optimized for broad range of applications including AI/ML, automotive, IoT, and defense

**MACsec Protocol Engines**
- Protects data in motion with robust Layer 2 security anchored in hardware
- Operates at full line-rate up to 800 Gbps supporting real-time applications
- Offers easy integration into networking SoCs and ASICs

**Provisioning and Key Management**
- Provision cryptographic information securely in untrusted environments
- Protects against cloning, reverse engineering, and counterfeiting
- Manufacturers can leverage securely provisioned keys and identities to enable supply chain integrity.
Silicon IP: Security

Protecting semiconductors and their secrets from design and manufacturing through deployment and end-of-life
Root of Trust

Portfolio of solutions from fully-programmable secure co-processors to highly compact state machines

- Provides hardware-based foundation for security
- Offers wide range of cryptographic functions and anti-tamper protections
800G MACsec Protocol Engine

- Protects data in motion with robust Layer 2 security anchored in hardware
- Operates at full line-rate up to 800 Gbps supporting real-time applications
- Offers easy integration into networking SoCs and ASICs

Multi-channel Protocol Engine Supports 100G to 800G MACsec
Thank you