This presentation contains forward-looking statements under the Private Securities Litigation Reform Act of 1995, including those relating to Rambus’ expectations regarding business opportunities, the Company’s ability to deliver ongoing long-term profitable growth, product and investment strategies, the Company’s outlook and financial guidance for the third quarter of 2021, and related drivers.

Such forward-looking statements are based on current expectations, estimates and projections, management’s beliefs and certain assumptions made by the Company’s management. Actual results may differ materially. The Company’s business generally is subject to a number of risks which are described more fully in Rambus’ periodic reports filed with the Securities and Exchange Commission, as well as the potential adverse impacts related to, or arising from, the Novel Coronavirus (COVID-19). The Company undertakes no obligation to update forward-looking statements to reflect events or circumstances after the date hereof.

Effective January 1, 2018, the Company adopted Accounting Standards Update No. 2014-09, Revenue from Contracts with Customers in ASC 606. The adoption of ASC 606 materially impacted the timing of revenue recognition for the Company’s fixed-fee intellectual property licensing arrangements. The adoption of ASC 606 did not have a material impact on the Company’s other revenue streams, net cash provided by operating activities, or its underlying financial position.

This presentation contains non-GAAP financial measures, including operating costs and expenses, interest and other income (expense), net and diluted net income (loss) per share. In computing these non-GAAP financial measures, stock-based compensation expenses, acquisition-related transaction costs and retention bonus expense, amortization expenses, depreciation expense on unused Electronic Design Automation (“EDA”) software licenses, expense on abandoned operating leases, restatement and shareholder activist costs, facility restoration costs, non-cash interest expense and certain other one-time adjustments were considered. The non-GAAP financial measures should not be considered a substitute for, or superior to, financial measures calculated in accordance with GAAP, and the financial results calculated in accordance with GAAP and reconciliations from these results should be carefully evaluated. Management believes the non-GAAP financial measures are appropriate for both its own assessment of, and to show investors, how the Company’s performance compares to other periods. Reconciliation from GAAP to non-GAAP results are made available and more fully described on our website as well as the back of this deck and in the earnings release.
Rambus at a Glance

- **Improving data bandwidth, capacity and security**
- **30+ Years**
  - Tech leadership & innovation
- **HQ in California**
  - with offices WW in India, EU and Asia
- **~600 Employees Worldwide**
- **Continued Innovation**
  - feeds licensing and product roadmap
- **3000+ Patents and Applications**
- **Pioneer of industry-leading chips and silicon IP making data faster and safer**
- **YoY Revenue Growth**
  - from Products, Contract and Other*
  - 41%
- **2020**
  - Cash from Operations
  - $185.5M
- **Strong balance sheet and cash generation fuel strategic initiatives**
- **Data Center**
  - 75%+
  - revenue from Data Center & Edge
  - *Includes Product and Contract & Other
- **Tech leadership & innovation**
- **30+ Years**
- **~600 Employees Worldwide**

*Excludes discontinued businesses
MORE AND MORE DATA
Data usage growing at 35% CAGR to 175ZB by 2025, driving overall server unit growth up 8% per year

ACCELERATING SHIFT TO CLOUD
Cloud driving Data Center growth, with equipment spend at top 5 hyperscalers doubling to $100B by 2024

GROWING AI/ML ADOPTION
Over 25% of server shipments in 2025 will be AI-specific with $10B in AI silicon

PROCESSING AT THE EDGE
Edge workloads increasing by 34% per year leading to $5B in Edge silicon by 2024

SECURITY THREATS ON THE RISE
Total number of DDoS attacks projected to double from 7.9M in 2018 to 15.4M in 2023

INCREASING CONNECTIVITY
In 2021, there were 27B connected smart devices capturing and sending data, up 10B over 5 years

HARDWARE SECURITY IS MISSION CRITICAL TO PROTECT VALUABLE DATA

Source: IDC, 650 Group, Cisco, MarketsandMarkets
Amplified Market Opportunity
Increasing need for bandwidth and security

FORECASTED ANNUAL GROWTH*

Market

↑ 4.5%: Data Center

Exponential rise in data usage driving secular growth

System

↑ 8%: Server Units

Rising AI/ML workloads driving server growth

Chip

↑ 26%: Server DRAM Bits

Need for more data driving memory bandwidth and bit growth

*Source: Arizton, IDC, Gartner
Semiconductor Industry Ecosystem Built on Leading-Edge IP

Markets
- Data Center
- 5G/Edge
- IoT
- Automotive
- Government

Cloud Providers
- Google
- Amazon
- Facebook
- Microsoft
- Alibaba Group

System OEMs
- HP
- Dell
- Quantas Computer
- Bosch
- Ericsson

Chip Makers
- Micron
- Samsung
- SK Hynix
- AMD
- Qualcomm
- Intel

Foundry
- TSMC
- Samsung
- Global Foundries

Technology Suppliers
- Renesas
- Mentor Technology
- Rambus
- Cadence
- Synopsys
- ARM

Ecosystem Example
Rambus Memory Interface Chip Growth

2018-2020

72% CAGR
Rambus Product Revenue (~Chips)

• Robust server memory demand projected 2021 and 2022
• Enhanced qualification footprint on new DDR4 platforms
• Strong market position on DDR5 platforms, shipping production orders
• Active ecosystem engagement on new memory architectures

Data • Faster • Safer
New Memory Architectures Driving TAM Expansion

Transition to DDR5

Memory Subsystem Expansion with Serial Links (e.g., CXL)

Data Center Disaggregation

Increasing bandwidth, capacity, efficiency and security
CXL Memory Interconnect Initiative

- Establishes focused development effort on breakthrough solutions for memory expansion and pooling for advanced data center architectures
- Complements existing memory interface chip business and leverages in-house expertise in high-speed I/O, memory and security

Expansion provides more main memory to Host (CPU) for higher performance on high-capacity workloads

Pooling provides additional main memory to Hosts on an “as needed” basis, improving performance, efficiency and TCO. Pooling ultimately supports disaggregation and composability.
Strategic Investments to Amplify Market Position

**Announcement to launch CXL Memory Interconnect research and development**

Rambus Advances New Era of Data Center Architecture with CXL™ Memory Interconnect Initiative

Highlights:
- Launches research and development effort to drive architectural shift in data centers with solutions for memory expansion and pooling that enable disaggregated and composable server architectures
- Combines unique expertise in high-speed interfaces, embedded security and server memory buffers to develop breakthrough solutions for next-generation data centers
- Leverages critical building blocks to be provided by PLDA and AnalogX acquisitions, accelerating CXL roadmap and market leadership

SAN JOSE, Calif. – June 16, 2021 – Rambus Inc. (NASDAQ:RMBS) a provider of industry-leading chips and silicon IP making data faster and safer, today announced the CXL Memory Interconnect Initiative to define and develop semiconductor solutions for advanced data center architectures that maximize performance, improve efficiency and reduce system cost. To support the continuing growth and specialization in server workloads, data center is moving to disaggregated architectures composed from shared and scalable pools of computing and memory resources. Compute Express Link™ (CXL) is a critical enabler of these next-generation disaggregated server architectures.

**Announcement of agreement to acquire leading CXL and PCIe digital controller provider, PLDA**

Rambus to Acquire PLDA, Extending Leadership with Cutting-Edge CXL™ and PCI Express® Digital IP

Highlights:
- Expands digital controller IP portfolio with complementary CXL 2.0, PCIe 5.0 and 6.0 controller and switch IP
- Enables integrated interface subsystem solutions for data center, artificial intelligence and machine learning (AI/ML), and High Performance Computing (HPC)
- Provides critical building blocks for Rambus CXL Memory interconnect initiative to advance high-bandwidth connectivity

SAN JOSE, Calif. – June 16, 2021 – Rambus Inc. (NASDAQ:RMBS) a provider of industry-leading chips and silicon IP making data faster and safer, today announced it has signed an agreement to acquire PLDA, an industry leader in Compute Express Link (CXL) and PCI Express (PCIe) digital solutions. The industry is on the verge of a groundbreaking shift to disaggregated data center architectures that promise to dramatically improve performance, efficiency and cost of ownership. CXL and PCIe will be critical enablers for these next-generation systems, delivering the high-speed interconnects between processors, accelerators, memory and network devices needed to tackle demanding workloads in AI/ML and HPC applications. With the addition of the world-class digital IP and engineering expertise from PLDA, Rambus will further its leadership in these mission critical interconnect chips and IP solutions for the future data center.

**Announcement of agreement to acquire leading high-speed, low-power PHY provider, AnalogX**

Rambus to Acquire AnalogX, Accelerating Next-Generation Data Center Interface Solutions

Highlights:
- Extends leadership in PCIe® 5.0 and 32G Multi-protocol SerDes with ultra-low power interface IP
- Accelerates time to market and enhances our roadmap for PAM4-based PCIe 6.0 and CXL™ 3.0 solutions for data center, artificial intelligence and machine learning (AI/ML), 5G and High Performance Computing (HPC)
- Provides critical building blocks for Rambus CXL Memory Interconnect Initiative to advance high-bandwidth connectivity

SAN JOSE, Calif. – June 16, 2021 – Rambus Inc. (NASDAQ:RMBS) a provider of industry-leading chips and silicon IP making data faster and safer, today announced it has signed an agreement to acquire AnalogX, the leading provider of low power multi-standard connectivity SerDes IP solutions. This acquisition augments the Rambus family of PCIe 5.0 and 32G Multi-protocol PHYs with SerDes technology specifically built for ultra-low power and very low latency, expanding the addressable applications and available process nodes. AnalogX’s expertise in DSP-based design and PAM4 signaling accelerates the Rambus roadmap for PCIe 6.0 and CXL 3.0 solutions and will provide critical building blocks for the CXL Memory Interconnect Initiative.
Rambus Delivers Fast and Secure Connections for Data Center

- Memory and SerDes IP: Accelerate data for AI
- Memory Interface Chips: Improve memory subsystem speed and capacity
- Secure Silicon IP: Protect valuable data

- Faster Data Rates
- Greater Capacity
- Higher Security
- Easy Integration
- Reliable Supplier
Product Leadership Driving Topline Growth

2018-2020

41% CAGR
Chip and Silicon IP combined revenue

Industry’s first DDR5 memory interface chips

Integrated PCIe5, HBM2E and GDDR6 memory PHY + Controller subsystems

Broadest portfolio of secure root of trust, protocol engine, and crypto accelerator cores

Experts in interface solutions critical for performance and utilization in emerging data center architectures
Financial Highlights

Chip & Silicon IP Revenue* ($M)

<table>
<thead>
<tr>
<th>Year</th>
<th>Chip &amp; Silicon IP</th>
<th>Discontinued Business</th>
</tr>
</thead>
<tbody>
<tr>
<td>2018</td>
<td>101</td>
<td>31</td>
</tr>
<tr>
<td>2019</td>
<td>133</td>
<td>19</td>
</tr>
<tr>
<td>2020</td>
<td>162</td>
<td></td>
</tr>
</tbody>
</table>

Pro Forma Operating Expenses ($M)

<table>
<thead>
<tr>
<th>Year</th>
<th>R&amp;D</th>
<th>SG&amp;A</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>2018</td>
<td>89</td>
<td>146</td>
<td>235</td>
</tr>
<tr>
<td>2019</td>
<td>80</td>
<td>144</td>
<td>224</td>
</tr>
<tr>
<td>2020</td>
<td>69</td>
<td>123</td>
<td>192</td>
</tr>
</tbody>
</table>

Cash from Operations ($M) & FCF per Share ($)

<table>
<thead>
<tr>
<th>Year</th>
<th>Cash from Ops</th>
<th>FCF per Share</th>
</tr>
</thead>
<tbody>
<tr>
<td>2018</td>
<td>86</td>
<td>0.68</td>
</tr>
<tr>
<td>2019</td>
<td>129</td>
<td>1.02</td>
</tr>
<tr>
<td>2020</td>
<td>186</td>
<td>1.26</td>
</tr>
</tbody>
</table>

Cash Equivalents & Return of Capital ($M)

<table>
<thead>
<tr>
<th>Year</th>
<th>Cash Equivalents</th>
<th>Return of Capital</th>
</tr>
</thead>
<tbody>
<tr>
<td>2018</td>
<td>278</td>
<td>50</td>
</tr>
<tr>
<td>2019</td>
<td>408</td>
<td>50</td>
</tr>
<tr>
<td>2020</td>
<td>503</td>
<td>50</td>
</tr>
</tbody>
</table>

*Includes Product and Contract & Other Revenue
Rambus Investment Summary

- Amplified market opportunity in data center as memory importance increases
- Pioneer of industry-leading chips and silicon IP enabling critical performance improvements for data center and cloud
- Continued innovation feeds patent portfolio and product roadmap expansion
- Focus on strategic initiatives drives financial results and profitable growth
- Strong cash generation enables strategic initiatives and return of capital to shareholders
Detailed Financials
### Continued Strong Cash Generation

<table>
<thead>
<tr>
<th>In Millions</th>
<th>ASC 606 Q2 2020</th>
<th>ASC 606 Q3 2020</th>
<th>ASC 606 Q4 2020</th>
<th>ASC 606 Q1 2021</th>
<th>ASC 606 Q2 2021</th>
</tr>
</thead>
<tbody>
<tr>
<td>Revenue</td>
<td>$61.7</td>
<td>$56.9</td>
<td>$61.9</td>
<td>$70.4</td>
<td>$84.9</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Balanced portfolio drives growth</td>
</tr>
<tr>
<td>Total Operating Costs and Expenses¹</td>
<td>$59.5</td>
<td>$56.7</td>
<td>$55.8</td>
<td>$58.2</td>
<td>$56.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Disciplined expense management through focus on core growth initiatives</td>
</tr>
<tr>
<td>Operating Income¹</td>
<td>$2.2</td>
<td>$0.2</td>
<td>$6.1</td>
<td>$12.1</td>
<td>$28.8</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Operating results under ASC 606 do not reflect significant cash flows from fixed-fee licensing arrangements</td>
</tr>
<tr>
<td>Cash from Operations</td>
<td>$62.0</td>
<td>$44.1</td>
<td>$42.1</td>
<td>$39.5</td>
<td>$51.6</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Sustained, predictable cash generation</td>
</tr>
</tbody>
</table>

¹Please refer to reconciliations of non-GAAP financial measures included in this presentation and in our earnings release.
## Solid Balance Sheet Supports Strategic Initiatives

<table>
<thead>
<tr>
<th></th>
<th>Q2 2020</th>
<th>Q3 2020</th>
<th>Q4 2020</th>
<th>Q1 2021</th>
<th>Q2 2021</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Total Cash &amp; Marketable Securities</strong></td>
<td>$486.1</td>
<td>$520.2</td>
<td>$502.6</td>
<td>$529.1</td>
<td>$477.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Driven by continued strong cash from operations</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Consistent capital return ($50M ASR in Q4 2020, $100M ASR in Q2 2021)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Total Assets</strong></td>
<td>$1,324.1</td>
<td>$1,316.6</td>
<td>$1,251.4</td>
<td>$1,235.8</td>
<td>$1,153.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Strong balance sheet with limited debt</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$324M and $345M contract assets in Q2 2021 and Q1 2021, respectively, related to ASC 606 adoption</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Stockholders’ Equity</strong></td>
<td>$972.7</td>
<td>$965.8</td>
<td>$912.7</td>
<td>$909.4</td>
<td>$830.6</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sustained, predictable cash generation</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## Reconciliation of Non-GAAP Financial Measures

### Net Income (Loss) in Millions

<table>
<thead>
<tr>
<th></th>
<th>Q2 2020 (ASC 606)</th>
<th>Q3 2020 (ASC 606)</th>
<th>Q4 2020 (ASC 606)</th>
<th>Q1 2021 (ASC 606)</th>
<th>Q2 2021 (ASC 606)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GAAP Net Income (loss)</td>
<td>($9)</td>
<td>($13)</td>
<td>($12)</td>
<td>($3)</td>
<td>$11</td>
</tr>
<tr>
<td>Adjustments:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Stock-based compensation</td>
<td>$7</td>
<td>$7</td>
<td>$6</td>
<td>$7</td>
<td>$7</td>
</tr>
<tr>
<td>Acquisition-related costs and retention bonus expense</td>
<td>$2</td>
<td>$1</td>
<td>$1</td>
<td>$1</td>
<td>$2</td>
</tr>
<tr>
<td>Amortization of acquired intangible assets</td>
<td>$5</td>
<td>$5</td>
<td>$5</td>
<td>$5</td>
<td>$5</td>
</tr>
<tr>
<td>Restructuring and other charges</td>
<td>$0</td>
<td>$0</td>
<td>$3</td>
<td>$0</td>
<td>$0</td>
</tr>
<tr>
<td>Non-cash interest expense</td>
<td>$2</td>
<td>$2</td>
<td>$2</td>
<td>$2</td>
<td>$2</td>
</tr>
<tr>
<td>Facility restoration costs</td>
<td>$0</td>
<td>$0</td>
<td>$0</td>
<td>$0</td>
<td>$0</td>
</tr>
<tr>
<td>Depreciation expense on unused EDA software licenses</td>
<td>$0</td>
<td>$0</td>
<td>$2</td>
<td>$0</td>
<td>$0</td>
</tr>
<tr>
<td>Expense on abandoned operating leases</td>
<td>$0</td>
<td>$0</td>
<td>$0</td>
<td>$1</td>
<td>$1</td>
</tr>
<tr>
<td>Restatement and shareholder activist costs</td>
<td>$0</td>
<td>$0</td>
<td>$0</td>
<td>$3</td>
<td>$0</td>
</tr>
<tr>
<td>Provision for (benefit from) income taxes</td>
<td>($1)</td>
<td>$0</td>
<td>($0)</td>
<td>($4)</td>
<td>($5)</td>
</tr>
<tr>
<td>Non-GAAP Net Income</td>
<td>$5</td>
<td>$2</td>
<td>$6</td>
<td>$11</td>
<td>$23</td>
</tr>
</tbody>
</table>

### Operating Income (Loss) in Millions

<table>
<thead>
<tr>
<th></th>
<th>Q2 2020 (ASC 606)</th>
<th>Q3 2020 (ASC 606)</th>
<th>Q4 2020 (ASC 606)</th>
<th>Q1 2021 (ASC 606)</th>
<th>Q2 2021 (ASC 606)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GAAP Operating Income (loss)</td>
<td>($11)</td>
<td>($13)</td>
<td>($11)</td>
<td>($3)</td>
<td>$14</td>
</tr>
<tr>
<td>Adjustments:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
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<td>$7</td>
<td>$6</td>
<td>$7</td>
<td>$7</td>
</tr>
<tr>
<td>Acquisition-related costs and retention bonus expense</td>
<td>$2</td>
<td>$1</td>
<td>$1</td>
<td>$1</td>
<td>$2</td>
</tr>
<tr>
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<td>$5</td>
<td>$5</td>
<td>$5</td>
<td>$5</td>
<td>$5</td>
</tr>
<tr>
<td>Restructuring and other charges</td>
<td>$0</td>
<td>$0</td>
<td>$3</td>
<td>$0</td>
<td>$0</td>
</tr>
<tr>
<td>Facility restoration costs</td>
<td>$0</td>
<td>$0</td>
<td>$0</td>
<td>$0</td>
<td>$0</td>
</tr>
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<td>$0</td>
<td>$2</td>
<td>$0</td>
<td>$0</td>
</tr>
<tr>
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<td>$0</td>
<td>$0</td>
<td>$0</td>
<td>$1</td>
<td>$1</td>
</tr>
<tr>
<td>Restatement and shareholder activist costs</td>
<td>$0</td>
<td>$0</td>
<td>$0</td>
<td>$3</td>
<td>$0</td>
</tr>
<tr>
<td>Provision for (benefit from) income taxes</td>
<td>($1)</td>
<td>$0</td>
<td>($0)</td>
<td>($4)</td>
<td>($5)</td>
</tr>
<tr>
<td>Non-GAAP Operating Income</td>
<td>$2</td>
<td>$0</td>
<td>$6</td>
<td>$12</td>
<td>$29</td>
</tr>
<tr>
<td>Depreciation</td>
<td>$5</td>
<td>$5</td>
<td>$7</td>
<td>$5</td>
<td>$5</td>
</tr>
<tr>
<td>Adjusted EBITDA</td>
<td>$7</td>
<td>$5</td>
<td>$13</td>
<td>$17</td>
<td>$34</td>
</tr>
</tbody>
</table>

Certain amounts may be off $1.0M due to rounding.
# Revenue and Licensing Billings

<table>
<thead>
<tr>
<th>In Thousands</th>
<th>ASC 606</th>
<th>ASC 606</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Q1’20</td>
<td>Q2’20</td>
</tr>
<tr>
<td>Royalty Revenue</td>
<td>$21,482</td>
<td>$18,744</td>
</tr>
<tr>
<td>Product Revenue</td>
<td>$30,728</td>
<td>$31,725</td>
</tr>
<tr>
<td>Contract and Other Revenue</td>
<td>$13,567</td>
<td>$11,248</td>
</tr>
<tr>
<td>Total</td>
<td>$65,777</td>
<td>$61,717</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>In Thousands</th>
<th>Q1’20</th>
<th>Q2’20</th>
<th>Q3’20</th>
<th>Q4’20</th>
<th>FY 2020</th>
<th>Q1’21</th>
<th>Q2’21</th>
<th>Q2’21 YTD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Royalty Revenue</td>
<td>$21,482</td>
<td>$18,744</td>
<td>$16,602</td>
<td>$27,732</td>
<td>$84,560</td>
<td>$28,859</td>
<td>$41,910</td>
<td>$70,769</td>
</tr>
<tr>
<td>Licensing Billings¹</td>
<td>$67,072</td>
<td>$60,687</td>
<td>$63,135</td>
<td>$64,195</td>
<td>$255,089</td>
<td>$63,506</td>
<td>$65,216</td>
<td>$128,722</td>
</tr>
<tr>
<td>Delta</td>
<td>$45,590</td>
<td>$41,943</td>
<td>$46,533</td>
<td>$36,463</td>
<td>$170,529</td>
<td>$34,647</td>
<td>$23,306</td>
<td>$57,953</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>In Thousands</th>
<th>Q1’20</th>
<th>Q2’20</th>
<th>Q3’20</th>
<th>Q4’20</th>
<th>FY 2020</th>
<th>Q1’21</th>
<th>Q2’21</th>
<th>Q2’21 YTD</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASC 606 Interest Income²</td>
<td>$4,437</td>
<td>$3,788</td>
<td>$3,379</td>
<td>$2,984</td>
<td>$14,588</td>
<td>$2,842</td>
<td>$2,382</td>
<td>$5,224</td>
</tr>
</tbody>
</table>

¹ Licensing billings is an operational metric that reflects amounts invoiced to our patent and technology licensing customers during the period, as adjusted for certain differences.

² Interest income associated with the significant financing component of licensing agreements as a result of the adoption of ASC 606.
## GAAP to Non-GAAP Income Statement

The following table reconciles GAAP to Non-GAAP financial metrics for Q2'21. Certain amounts may be off $0.1M due to rounding.

<table>
<thead>
<tr>
<th>In $ Millions</th>
<th>GAAP Actual Q2'21</th>
<th>Non-GAAP Actual Q2'21</th>
<th>Delta to GAAP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Revenue</td>
<td>$84.9</td>
<td>$84.9</td>
<td>$-</td>
</tr>
<tr>
<td>Cost of revenue</td>
<td>16.9</td>
<td>12.4</td>
<td>(4.5)</td>
</tr>
<tr>
<td>Research and development</td>
<td>31.5</td>
<td>28.1</td>
<td>(3.4)</td>
</tr>
<tr>
<td>Sales, general and administrative</td>
<td>22.4</td>
<td>15.6</td>
<td>(6.8)</td>
</tr>
<tr>
<td>Total operating cost and expenses</td>
<td>70.8</td>
<td>56.1</td>
<td>(14.7)</td>
</tr>
<tr>
<td>Operating income</td>
<td>14.1</td>
<td>28.8</td>
<td>14.7</td>
</tr>
<tr>
<td>Interest and other income (expense), net</td>
<td>(0.3)</td>
<td>1.6</td>
<td>1.9</td>
</tr>
<tr>
<td>Income before income taxes</td>
<td>13.8</td>
<td>30.4</td>
<td>16.6</td>
</tr>
<tr>
<td>Provision for income taxes</td>
<td>2.6</td>
<td>7.3</td>
<td>4.6</td>
</tr>
<tr>
<td>Net income</td>
<td>$11.2</td>
<td>$23.1</td>
<td>$11.9</td>
</tr>
</tbody>
</table>
Product Overview
Semiconductor Solutions Built on Leading-Edge IP

Architecture License
- Foundational IP

Silicon IP
- Security IP: Secure Cores and Provisioning
- Interface IP: Memory and SerDes PHYs and Controllers

Chips
- Memory Interface Chips
Innovating to Meet Market Needs

Growing Patent Portfolio

- **Fundamental R&D feeds product development**
- **Relevant portfolio regularly cited by major industry players**
- **Supports predictable licensing base and sustained cash generation**

Industry Recognition of Rambus Patents

Source: Innography, patent citations
Memory Interface Chips
Built for speed, power efficiency and reliability, the DDRn memory interface chips for RDIMM, LRDIMM and NVDIMM server modules deliver top-of-the-line performance and the capacity needed to meet the growing demands on enterprise and data center systems.

Industry-leading Performance
• Fully-compliant with the latest JEDEC standards
• Operational speeds up to 4800 Mbps

Enhanced Margin
• Wide margin I/O design with advanced programmability
• Exceed JEDEC reliability standards for ESD and EOS

Optimized Power
• Advanced power management
• Frequency-based, low-power optimization

Superior Debug and Serviceability
• Integrated tools for bring-up and debug
• Works out-of-the-box with no BIOS changes required
Memory Interface Chips

Enabling performance and capacity in server DIMMs

**DDR5**
- DB & RCD
- Per JEDEC Direction
- Speeds of 4800 Mbps
- Ongoing qualifications
- AVAILABLE IN PRODUCTION

**DDR4**
- DB & RCD
- JEDEC Compliant
- Speeds up to 3200 Mbps
- Multiple OEM qualifications
- AVAILABLE IN PRODUCTION

**NV**
- DDR4 NVRC
- JEDEC Compliant
- Speeds up to 3200 Mbps
- Ongoing qualifications
- AVAILABLE IN PRODUCTION

**DDR3**
- DB & RCD
- JEDEC Compliant
- Speeds up to 2133 Mbps
- Multiple OEM qualifications
- AVAILABLE IN PRODUCTION

Smart tools for easy integration and reduced time to market

LabStation Platform and Buffer BIOS Integration Tool

Validated solutions with partners

SAMSUNG  SK hynix  Micron
DIMM Memory Interface chips reduce the number of loads to enable higher system capacity and performance.

Memory Interface Chips = RCD + DB

DDR5 Registered DIMM (RDIMM)

DDR5 Load Reduced DIMM (LRDIMM)
Across a broad spectrum of applications spanning automotive, artificial intelligence (AI), Internet of Things (IoT), network edge, and data center, there is a common need to move more data faster. Rambus memory and SerDes IP deliver the performance needed by the most demanding applications to move the data at blinding fast speeds.

**HBM2E Memory Subsystem**
- Fully-integrate and silicon-proven PHY and controller
- Running at industry’s fastest data rate up to 4.0 Gbps
- Ideal for AI/ML training, graphics and networking applications

**GDDR6 Memory Subsystem**
- Fully-integrate and silicon-proven PHY and controller
- Running at industry’s fastest data rate up to 18.0 Gbps
- Ideal for AI/ML interference, automotive, graphics and networking applications

**PCIe 5**
- Co-validated PHY and controller
- PHY supports Compute Express Link (CXL)
- Multiple configurations to support broad range of applications
# Memory Interface Solutions

## Memory PHY and digital controller solutions

<table>
<thead>
<tr>
<th>Memory Type</th>
<th>Speeds</th>
<th>Channels</th>
<th>Ranks</th>
<th>Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>HBM2E</td>
<td>3.6 Gbps</td>
<td>12-18 Gbps</td>
<td>1-4</td>
<td>7 &amp; 11nm</td>
</tr>
<tr>
<td>GDDR6</td>
<td>12-18 Gbps</td>
<td>2x 16-bit channels</td>
<td></td>
<td>7nm</td>
</tr>
<tr>
<td>DDR4/3</td>
<td>3200 Mbps</td>
<td>x16 to x72-bits</td>
<td>1-4</td>
<td>12 &amp; 28nm</td>
</tr>
</tbody>
</table>

- Easy-to-use PC Interface
- Interface to 3rd party software
- Pre-defined test scripts
- PHY control settings
- External instrument control
- System characteristics and analysis

**LabStation Platform**

**Verification tools**

- Easy-to-use PC Interface
- Interface to 3rd party software
- Pre-defined test scripts
- PHY control settings
- External instrument control
- System characteristics and analysis
Complete HBM2E Interface

Applications
- AI/ML
- Graphics
- Networking

Features
- JEDEC standard compliant
- 7nm process node
- 461 GB/s maximum bandwidth
- Speed bins to 3.6 Gbps with operation to 4.0 Gbps
- Support for stacks of 2, 4, 8 or 12 DRAM

HBM2E Memory Interface Subsystem (Controller & PHY)

World’s fastest HBM2E Operating at 4.0 Gbps
Complete GDDR6 Interface

Applications:
• AI/ML
• Automotive
• Graphics
• Networking

Features:
• JEDEC standard compliant
• 7nm process node
• 72 GB/s maximum bandwidth
• Speed Bins: 12, 14, 16, 18 Gbps
• Supported DRAM: 8, 12, 16 Gbit
• ASIC Interface: DFI style
• Supports clam shell mode
• All training and calibration modes support
# High-Speed SerDes Solutions

## SerDes PHY and digital controller solutions

<table>
<thead>
<tr>
<th>PCIe 5</th>
<th>CXL 2</th>
<th>40G</th>
<th>32G</th>
<th>28G</th>
</tr>
</thead>
<tbody>
<tr>
<td>CXL 2/1.1</td>
<td>7 &amp; 12 &amp; 22nm</td>
<td>C2C</td>
<td>40G USR</td>
<td>CEI-28/25/11</td>
</tr>
<tr>
<td>PCIe 4/3/2</td>
<td></td>
<td></td>
<td></td>
<td>40/10GbE</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>JESD204B/C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>CPRI</td>
</tr>
</tbody>
</table>

## Integrated tools for easy bring-up and characterization

- Easy-to-use PC Interface
- Interface to 3rd party software
- Pre-defined test scripts
- PHY control settings
- External instrument control
- System characteristics and analysis

## Verification tools

![avery design systems logo]
Complete PCIe 5.0 Interface

Co-validated PCIe 5 PHY and Controller

- Eases SoC integration effort
- Reduces design risk
- Speeds time to market

Features

- Backward compatible to PCIe 4/3/2
- PHY supports Compute Express Link (CXL)
- X1, X2, X4, X8 and X16 lane configuration support
- Supports >36dB of channel insertion loss
- Available in 7nm
Rambus secure silicon IP helps protect data at rest and in motion across a broad range of applications and throughout a device’s lifecycle. Securing electronic systems at their hardware foundation, our embedded security solutions span areas including root of trust, tamper resistance, content protection and trusted provisioning.

### Root of Trust Cores
- Portfolio of solutions from fully-programmable secure co-processors to highly-compact state machines
- Provides hardware-based foundation for security
- Optimized for broad range of applications including AI/ML, automotive, IoT and defense

### 800G MACSec Engine
- Protects data in motion with robust Layer 2 security anchored in hardware
- Operates at full line-rate up to 800 Gbps supporting real-time applications
- Offers easy integration into networking SoCs and ASICs

### Provisioning and Key Management
- Provision cryptographic information securely in untrusted environments
- Protect against cloning, reverse engineering, and counterfeiting
- Manufacturers can leverage securely provisioned keys and identities to enable supply chain integrity.
Silicon IP: Security

Protecting semiconductors and their secrets from design and manufacturing through deployment and end-of-life.

Secure Cores
- Root of Trust
- Protocol Engines
- Crypto Cores
- Anti-Counterfeiting

Secure Protocols

Secure Provisioning
- Key and Data Injection
- Device Key Management

End-to-End Security Solution
Root of Trust

Portfolio of solutions from fully-programmable secure co-processors to highly compact state machines
- Provides hardware-based foundation for security
- Offers wide range of cryptographic functions and anti-tamper protections

Secure processing is separated from general processing for greater protection

Secure Co-Processor Root of Trust (RT-600 Series)
800G MACsec Protocol Engine

- Protects data in motion with robust Layer 2 security anchored in hardware
- Operates at full line-rate up to 800 Gbps supporting real-time applications
- Offers easy integration into networking SoCs and ASICs

Multi-channel Protocol Engine Supports 100G to 800G MACsec
Thank you