This presentation contains forward-looking statements under the Private Securities Litigation Reform Act of 1995 including Rambus’ financial guidance for future periods, product and investment strategies, timing of expected product launches, demand for existing and newly-acquired technologies, the growth opportunities of the various markets we serve, the expected benefits of our merger, acquisition and divestiture activity, including the success of our integration efforts, and the effects of ASC 606 on reported revenue, amongst other things.

Such forward-looking statements are based on current expectations, estimates and projections, management’s beliefs and certain assumptions made by Rambus’ management. Actual results may differ materially. Our business is subject to a number of risks which are described more fully in our periodic reports filed with the Securities and Exchange Commission, as well risks and the potential adverse impacts related to, or arising from, the Novel Coronavirus (COVID-19). Rambus undertakes no obligation to update forward-looking statements to reflect events or circumstances after the date hereof.

Effective January 1, 2018, the Company adopted Accounting Standards Update No. 2014-09, Revenue from Contracts with Customers in ASC 606. The adoption of ASC 606 materially impacted the timing of revenue recognition for the Company's fixed-fee intellectual property licensing arrangements. The adoption of ASC 606 did not have a material impact on the Company's other revenue streams, net cash provided by operating activities, or its underlying financial position.

This presentation contains non-GAAP financial measures, including operating costs and expenses, interest and other income (expense), net and diluted net income (loss) per share. In computing these non-GAAP financial measures, stock-based compensation expenses, acquisition-related transaction costs and retention bonus expense, amortization expenses, non-cash interest expense and certain other one-time adjustments were considered. The non-GAAP financial measures should not be considered a substitute for, or superior to, financial measures calculated in accordance with GAAP, and the financial results calculated in accordance with GAAP and reconciliations from these results should be carefully evaluated. Management believes the non-GAAP financial measures are appropriate for both its own assessment of, and to show investors, how the Company’s performance compares to other periods. Reconciliation from GAAP to non-GAAP results are made available and more fully described on our website as well as the back of this deck and in the earnings release.
Rambus at a Glance

Who We Are

- Premier silicon IP and chip provider, making data faster and safer
- Developed foundational technology for all modern computing systems
- Improving performance, capacity and security for leading SoCs and systems

Rambus Offerings

<table>
<thead>
<tr>
<th>Architecture Licenses</th>
<th>High-speed IO &amp; DPA Countermeasures</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon IP</td>
<td>High-speed Interface and Security IP</td>
</tr>
<tr>
<td>Chips</td>
<td>Memory Interface Chips</td>
</tr>
</tbody>
</table>

Financial Performance

<table>
<thead>
<tr>
<th></th>
<th>Q120</th>
<th>2019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Licensing Billings</td>
<td>$67.1M</td>
<td>$267.2M</td>
</tr>
<tr>
<td>Contract &amp; Other Revenue</td>
<td>$13.6M</td>
<td>$60.3M</td>
</tr>
<tr>
<td>Product Revenue</td>
<td>$30.7M</td>
<td>$73.0M</td>
</tr>
<tr>
<td>Cash from Operations</td>
<td>$37.3M</td>
<td>$128.5M</td>
</tr>
</tbody>
</table>

NASDAQ: RMBS

30 Years Tech leadership & innovation

2900+ Patents and Applications

HQ: California

WW Offices in India, EU, Asia

~700 Employees Worldwide
Targeting Growth Markets

Artificial Intelligence
- Accurate training requires enormous amounts of data - memory bandwidth is key. Securing training and inference models and data now vital

Data Center
- Explosion of data pushing demands on interconnects to move data faster. Value of data demands securing the communication links

Autonomous/ADAS Automotive
- Real-time decisions from multiple inputs increase demand on processing and trust in the data

Edge Compute (5G)
- Near edge (base stations) drive performance and far edge (gateways and routers) demand power efficiency and trust

Internet of Things
- Billions of connected endpoints make device-level security critical to enabling trust across the ecosystem

Defense
- Trusted device authentication is critical to global supply chain
Semiconductor Industry Ecosystem Built on Leading-Edge IP

Markets
- AI/ML
- Data Center
- Automotive
- Communications
- IoT
- Government

Cloud Providers
- Google
- amazon
- facebook
- Microsoft
- Alibaba Group

System OEMs
- hp
- DELL
- HTC
- ERICSSON

Chip Makers
- Micron
- SAMSUNG
- SK hynix
- QUALCOMM
- Intel

Foundry
- tsmc
- GLOBAL FOUNDRIES
- SAMSUNG

Technology Suppliers
- RENESAS
- MONTAGE TECHNOLOGY
- Inphi
- Rambus
- cadence
- synopsys
- arm

Ecosystem Example
Semiconductor Solutions Built on Leading-Edge IP

**Architecture License**
- Foundational IP

**Silicon IP**
- Security IP: Secure Cores, Protocols and Provisioning
- Interface IP: Memory and SerDes PHYs and Controllers

**Chips**
- Memory Interface Chips
Strong, Growing and Relevant Patent Portfolio

Growing patent portfolio in key areas:
- Memory architectures
- High-speed serial links
- Embedded security

Relevant portfolio regularly cited by major industry players

Source: IHS Markit and Innography, respectively
Products Driving Growth

Record Q1’20 revenue for Silicon IP and Chips

Product Revenue ($M)

- **Contract & Other (~Silicon IP)**
  - Q120 Up 84% over Q119 to $13.6M

- **Product (~Chips)**
  - Q120 > 3X revenue of Q119 at $30.7M
## Continued Strong Cash Generation

<table>
<thead>
<tr>
<th>In Millions</th>
<th>ASC 606 Q1 2019</th>
<th>ASC 606 Q2 2019</th>
<th>ASC 606 Q3 2019</th>
<th>ASC 606 Q4 2019</th>
<th>ASC 606 Q1 2020</th>
</tr>
</thead>
<tbody>
<tr>
<td>Revenue</td>
<td>$48.4</td>
<td>$58.3</td>
<td>$57.4</td>
<td>$59.9</td>
<td>$64.0</td>
</tr>
<tr>
<td>Year over year growth from chip and Silicon IP revenue. Impacted by structure and timing of key licensing arrangements.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total Operating Expenses&lt;sup&gt;1&lt;/sup&gt;</td>
<td>$67.3</td>
<td>$64.1</td>
<td>$67.1</td>
<td>$62.3</td>
<td>$63.5</td>
</tr>
<tr>
<td>Managed expenses through refocus on core growth initiatives.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Income (Loss)&lt;sup&gt;1&lt;/sup&gt;</td>
<td>($18.9)</td>
<td>($5.8)</td>
<td>($9.7)</td>
<td>($2.3)</td>
<td>$0.5</td>
</tr>
<tr>
<td>Operating results under ASC 606 do not reflect significant cash flow from fixed-fee licensing arrangements</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cash from Operations</td>
<td>$28.8</td>
<td>$38.7</td>
<td>$25.6</td>
<td>$35.4</td>
<td>$37.3</td>
</tr>
<tr>
<td>Outstanding cash generation</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<sup>1</sup>Please refer to reconciliations of non-GAAP financial measures included in this presentation and in our earnings release.
## Solid Balance Sheet Supports Strategic Initiatives

<table>
<thead>
<tr>
<th></th>
<th>Q1 2019</th>
<th>Q2 2020</th>
<th>Q3 2020</th>
<th>Q4 2019</th>
<th>Q1 2020</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Total Cash &amp; Markable Securities</strong></td>
<td>$305.9</td>
<td>$337.7</td>
<td>$338.0</td>
<td>$407.7</td>
<td>$435.4</td>
</tr>
<tr>
<td><strong>Total Assets</strong></td>
<td>$1,321.4</td>
<td>$1,312.2</td>
<td>$1,299.8</td>
<td>$1,339.0</td>
<td>$1,319.5</td>
</tr>
<tr>
<td><strong>Stockholders’ Equity</strong></td>
<td>$999.9</td>
<td>$973.2</td>
<td>$961.3</td>
<td>$970.9</td>
<td>$965.7</td>
</tr>
<tr>
<td><strong>Cash from Operations</strong></td>
<td>$28.8</td>
<td>$38.7</td>
<td>$25.6</td>
<td>$35.4</td>
<td>$37.3</td>
</tr>
</tbody>
</table>
Strong Cash From Operations

Low Capital Expenditure, Consistent Return to Shareholders

- Execution of strategy and operational discipline yields excellent cash flow
- Strong cash position enables flexibility for M&A
- Returned $200M of cash to shareholders from 2015 through 2018 through Accelerated Share Repurchase programs
Rambus Investment Summary

- Focusing on core strengths in semiconductor with unique expertise
- Growing patent portfolio of interface and security IP has continued relevance
- Strong balance sheet and cash generation to re-invest in R&D and M&A in areas of focus
- Delivering to performance-intensive, high-growth market segments including data center, edge, AI and automotive
Thank you
Reconcilation of Non-GAAP Financial Measures

<table>
<thead>
<tr>
<th>Net Income (Loss) in Millions</th>
<th>Q1 2019 (AC 606)</th>
<th>Q2 2019 (ASC 606)</th>
<th>Q3 2019 (ASC 606)</th>
<th>Q4 2019 (ASC 606)</th>
<th>Q1 2020 (ASC 606)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GAAP Net Loss</td>
<td>($27)</td>
<td>($37)</td>
<td>($17)</td>
<td>($10)</td>
<td>($8)</td>
</tr>
<tr>
<td>Adjustments:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Stock-based compensation</td>
<td>$7</td>
<td>$7</td>
<td>$7</td>
<td>$5</td>
<td>$6</td>
</tr>
<tr>
<td>Acquisition-related/divestiture costs</td>
<td>$0</td>
<td>$0</td>
<td>$3</td>
<td>$4</td>
<td>$2</td>
</tr>
<tr>
<td>Amortization</td>
<td>$5</td>
<td>$5</td>
<td>$3</td>
<td>$4</td>
<td>$5</td>
</tr>
<tr>
<td>Restructuring charges and other</td>
<td>$0</td>
<td>$3</td>
<td>$1</td>
<td>$5</td>
<td>$1</td>
</tr>
<tr>
<td>Non-cash interest expense</td>
<td>$2</td>
<td>$2</td>
<td>$2</td>
<td>$2</td>
<td>$2</td>
</tr>
<tr>
<td>Impairment (recovery) on assets held for sale</td>
<td>$0</td>
<td>$17</td>
<td>($2)</td>
<td>($8)</td>
<td>$0</td>
</tr>
<tr>
<td>Escrow settlement refund</td>
<td>$0</td>
<td>($0)</td>
<td>$0</td>
<td>$0</td>
<td>$0</td>
</tr>
<tr>
<td>Facility restoration costs</td>
<td>$0</td>
<td>$0</td>
<td>$0</td>
<td>$1</td>
<td>$0</td>
</tr>
<tr>
<td>Change in fair value of earn-out liability</td>
<td>$0</td>
<td>$0</td>
<td>$0</td>
<td>$0</td>
<td>($2)</td>
</tr>
<tr>
<td>Provision for (benefit from) income taxes</td>
<td>$3</td>
<td>$4</td>
<td>($0)</td>
<td>($1)</td>
<td>($1)</td>
</tr>
<tr>
<td>Non-GAAP Net Income (Loss)</td>
<td>($9)</td>
<td>$1</td>
<td>($3)</td>
<td>$2</td>
<td>$5</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Operating Income (Loss) in Millions</th>
<th>Q1 2019 (AC 606)</th>
<th>Q2 2019 (ASC 606)</th>
<th>Q3 2019 (ASC 606)</th>
<th>Q4 2019 (ASC 606)</th>
<th>Q1 2020 (ASC 606)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GAAP Operating Loss</td>
<td>($31)</td>
<td>($37)</td>
<td>($23)</td>
<td>($13)</td>
<td>($11)</td>
</tr>
<tr>
<td>Adjustments:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Stock-based compensation</td>
<td>$7</td>
<td>$7</td>
<td>$7</td>
<td>$5</td>
<td>$6</td>
</tr>
<tr>
<td>Acquisition-related/divestiture costs</td>
<td>$0</td>
<td>$0</td>
<td>$3</td>
<td>$4</td>
<td>$2</td>
</tr>
<tr>
<td>Amortization</td>
<td>$5</td>
<td>$5</td>
<td>$3</td>
<td>$4</td>
<td>$5</td>
</tr>
<tr>
<td>Restructuring and other charges</td>
<td>$0</td>
<td>$3</td>
<td>$1</td>
<td>$5</td>
<td>$1</td>
</tr>
<tr>
<td>Impairment (recovery) on assets held for sale</td>
<td>$0</td>
<td>$17</td>
<td>($2)</td>
<td>($8)</td>
<td>$0</td>
</tr>
<tr>
<td>Escrow settlement refund</td>
<td>$0</td>
<td>($0)</td>
<td>$0</td>
<td>$0</td>
<td>$0</td>
</tr>
<tr>
<td>Facility restoration costs</td>
<td>$0</td>
<td>$0</td>
<td>$0</td>
<td>$1</td>
<td>$0</td>
</tr>
<tr>
<td>Change in fair value of earn-out liability</td>
<td>$0</td>
<td>$0</td>
<td>$0</td>
<td>$0</td>
<td>($2)</td>
</tr>
<tr>
<td>Non-GAAP Operating Income (Loss)</td>
<td>($19)</td>
<td>($6)</td>
<td>($10)</td>
<td>($2)</td>
<td>$1</td>
</tr>
<tr>
<td>Depreciation</td>
<td>$3</td>
<td>$3</td>
<td>$4</td>
<td>$5</td>
<td>$5</td>
</tr>
<tr>
<td>Adjusted EBITDA</td>
<td>($16)</td>
<td>($3)</td>
<td>($5)</td>
<td>$3</td>
<td>$5</td>
</tr>
</tbody>
</table>
Revenue and Licensing Billings

<table>
<thead>
<tr>
<th>In Thousands</th>
<th>ASC 606</th>
<th>ASC 606</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Q1'19</td>
<td>Q2'19</td>
</tr>
<tr>
<td>Royalty Revenue</td>
<td>$24,853</td>
<td>$27,050</td>
</tr>
<tr>
<td>Product Revenue</td>
<td>$8,964</td>
<td>$16,031</td>
</tr>
<tr>
<td>Contract and Other Revenue</td>
<td>$14,567</td>
<td>$15,216</td>
</tr>
<tr>
<td>Total</td>
<td>$48,384</td>
<td>$58,297</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>In Thousands</th>
<th>Q1'19</th>
<th>Q2'19</th>
<th>Q3'19</th>
<th>Q4'19</th>
<th>FY 2019</th>
<th>Q1'20</th>
</tr>
</thead>
<tbody>
<tr>
<td>Royalty Revenue</td>
<td>$24,853</td>
<td>$27,050</td>
<td>$19,448</td>
<td>$19,434</td>
<td>$90,785</td>
<td>$19,694</td>
</tr>
<tr>
<td>Licensing Billings(^1)</td>
<td>$75,460</td>
<td>$64,948</td>
<td>$63,058</td>
<td>$63,758</td>
<td>$267,224</td>
<td>$67,072</td>
</tr>
<tr>
<td>Delta</td>
<td>$50,607</td>
<td>$37,898</td>
<td>$43,610</td>
<td>$44,324</td>
<td>$176,439</td>
<td>$47,378</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>In Thousands</th>
<th>Q1'19</th>
<th>Q2'19</th>
<th>Q3'19</th>
<th>Q4'19</th>
<th>FY 2019</th>
<th>Q1'20</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASC 606 Interest Income(^2)</td>
<td>$5,707</td>
<td>$5,288</td>
<td>$4,925</td>
<td>$4,469</td>
<td>$20,389</td>
<td>$4,368</td>
</tr>
</tbody>
</table>

\(^1\) Licensing billings is an operational metric that reflects amounts invoiced to our patent and technology licensing customers during the period, as adjusted for certain differences.

\(^2\) Interest income associated with the significant financing component of licensing agreements as a result of the adoption of ASC 606.
GAAP to Non-GAAP Income Statement

<table>
<thead>
<tr>
<th>In $ Millions</th>
<th>GAAP Actual Q1'20</th>
<th>Non-GAAP Actual Q1'20</th>
<th>Delta to GAAP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Revenue</td>
<td>$64.0</td>
<td>$64.0</td>
<td>$-</td>
</tr>
<tr>
<td>Cost of revenue</td>
<td>15.9</td>
<td>11.5</td>
<td>(4.4)</td>
</tr>
<tr>
<td>Research and development</td>
<td>36.7</td>
<td>32.8</td>
<td>(3.9)</td>
</tr>
<tr>
<td>Sales, general and administrative</td>
<td>23.2</td>
<td>19.1</td>
<td>(4.1)</td>
</tr>
<tr>
<td>Change in fair value of earn-out liability</td>
<td>(1.8)</td>
<td>0.0</td>
<td>1.8</td>
</tr>
<tr>
<td>Restructuring charges</td>
<td>0.8</td>
<td>0.0</td>
<td>(0.8)</td>
</tr>
<tr>
<td>Total operating cost and expenses</td>
<td>74.8</td>
<td>63.5</td>
<td>(11.3)</td>
</tr>
<tr>
<td>Operating income (loss)</td>
<td>(10.8)</td>
<td>0.5</td>
<td>11.3</td>
</tr>
<tr>
<td>Interest and other income (expense), net</td>
<td>3.8</td>
<td>5.6</td>
<td>1.8</td>
</tr>
<tr>
<td>Income (loss) before income taxes</td>
<td>(7.0)</td>
<td>6.1</td>
<td>13.1</td>
</tr>
<tr>
<td>Provision for income taxes</td>
<td>1.0</td>
<td>1.5</td>
<td>0.5</td>
</tr>
<tr>
<td>Net income (loss)</td>
<td>($8.0)</td>
<td>$4.7</td>
<td>$12.7</td>
</tr>
</tbody>
</table>

Certain amounts may be off $0.1M due to rounding.
Product Overview
Silicon IP
From chip-to-cloud, Rambus secure silicon IP helps protect the world’s most valuable resource: data. Securing electronic systems at their hardware foundation, our embedded security solutions span areas including secure co-processors, crypto accelerators, secure protocols, anti-counterfeiting and trusted provisioning.

**Improved Profitability**
- Improved time-to-market and reduced inventory waste
- Dynamic SKU and feature management lowers inventory costs
- Reduce revenue lost to unauthorized access and counterfeits

**Superior Security**
- Provide a robust hardware root-of-trust
- Secure valuable secret keys, identity credentials, intellectual property, and other sensitive data
- Protect against cloning, counterfeiting, and reverse engineering

**Managed Value Chain**
- Actively monitor production status, availability, and inventory levels
- Validate process information through secure logs
- Deploy in distributed, high-volume manufacturing
Silicon IP: Security

Protecting semiconductors and their secrets from design and manufacturing through deployment and end-of-life

Secure Cores
Secure Co-Processors
Protocol Engines
Crypto Cores
Anti-Counterfeiting

Secure Protocols

Secure Provisioning
Key and Data Injection
Device Key Management

End-to-End Security Solution
CryptoManager Root of Trust

Family of fully-programmable secure co-processors
- Protects private data (keys and chip identity) with security anchored in hardware
- Adapts to an evolving threat landscape
- Supports new secure features and applications

Purpose-built for security with defense in depth against attacks
800G MACsec Protocol Engine

- Protects data in motion with robust Layer 2 security anchored in hardware
- Operates at full line-rate up to 800 Gbps supporting real-time applications
- Secures the communication path from end devices to servers in the data center

Multi-channel Protocol Engine Supports 100G to 800G MACsec
Optimized for power and area, our line-up of SerDes Interface solutions deliver maximum performance and flexibility for today’s most challenging systems.

**Fully Standards-Compatible**
- Compliant with the latest industry-standard specifications
- Support for multi-modal functionality

**Enhanced Design Flexibility**
- Support for multiple packaging options
- Enhanced margin and yield

**Reduced Power**
- Improved power efficiency
- Lower signaling and stand-by power

**Improved Performance**
- Increased data rates
- Improved bandwidth
- Higher capacity
# High-Speed SerDes Solutions

## SerDes PHY and digital controller solutions

<table>
<thead>
<tr>
<th>16G</th>
<th>28G</th>
<th>PCIe 5</th>
<th>112G</th>
</tr>
</thead>
<tbody>
<tr>
<td>28nm &amp; 14nm</td>
<td>14nm</td>
<td>7nm</td>
<td>7nm</td>
</tr>
<tr>
<td>• PCIe 4/3/2</td>
<td>• CEI-28/25/11</td>
<td>• PCIe 5</td>
<td>• CEI-112G LR</td>
</tr>
<tr>
<td>• CEI 11/6</td>
<td>• 100/10GbE</td>
<td>• CXL (PHY)</td>
<td>• CEI-112G XSR</td>
</tr>
<tr>
<td>• XFI/XAUI</td>
<td>• FC28</td>
<td>• PCIe 4/3/2</td>
<td>• CEI-56/28/25</td>
</tr>
<tr>
<td>• SATA</td>
<td>• XFI/XAUI</td>
<td></td>
<td>• 800/400/200/100GbE</td>
</tr>
<tr>
<td>• SAS</td>
<td></td>
<td></td>
<td>• PAM-4/NRZ</td>
</tr>
</tbody>
</table>

*LEAD CUSTOMERS*

## Integrated tools for easy bring-up and characterization

- Easy-to-use PC Interface
- Interface to 3rd party software
- Pre-defined test scripts
- PHY control settings
- External instrument control
- System characteristics and analysis

**LabStation Platform**

## PCIe digital controllers

- Northwest Logic
  - a Rambus Company
Complete PCIe 5.0 Interface

Co-validated PCIe 5 PHY and Controller

- Eases SoC integration effort
- Reduces design risk
- Speeds time to market

Features

- Backward compatible to PCIe 4/3/2
- Supports Compute Express Link (CXL)
- X1, X2, X4, X8 and X16 lane configuration support
- Supports >36dB of channel insertion loss
- Available in 7nm
Silicon IP: Memory PHYs and Controllers

With their reduced power consumption and industry-leading data rates, our line-up of enhanced memory interface solutions support a broad range of industry standards with improved margin and flexibility.

**Fully Standards-Compatible**
- Compliant with the latest JEDEC and industry-standard specifications
- Support for multi-modal functionality

**Enhanced Design Flexibility**
- Support for multitude packaging options
- Enhanced margin and yield

**Reduced Power**
- Improved power efficiency
- Lower signaling and stand-by power

**Improved Performance**
- Increased data rates
- Improved bandwidth
- Higher capacity
Memory Interface Solutions

Memory PHY and digital controller solutions

**DDR4/3**
- 28nm & 14nm
- 3200 Mbps
- x16 to x72-bits
- 1-4 Ranks
- DFI 4.0

**HBM2**
- 14nm
- 2000 Mbps
- 1024-bit
- 2.5D design architecture

**GDDR6**
- 12-18 Gbps
- 2x 16-bit channels

**DDR5 & HBM3**

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**Integrated tools for easy bring-up and characterization**

- Easy-to-use PC Interface
- Interface to 3rd party software
- Pre-defined test scripts
- PHY control settings
- External instrument control
- System characteristics and analysis

**LabStation Platform**

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**Memory digital controllers**

**ROADMAP**

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Data • Faster • Safer

**Northwest Logic**
a Rambus Company
Complete GDDR6 Interface

Applications:
- AI/ML
- Automotive
- Graphics
- Networking

Features:
- JEDEC standard compliant
- 7nm process node
- 72 GB/s maximum bandwidth
- Speed Bins: 12, 14, 16, 18 Gbps
- Supported DRAM: 8, 12, 16 Gbit
- ASIC Interface: DFI style
- Supports clam shell mode
- All training and calibration modes support

GDDR6 Memory Interface Subsystem
(Controller + PHY)

GDDR6 18 Gbps Transmit Eye
Complete HBM2E Interface

Applications
- AI/ML
- Graphics
- Networking

Features
- JEDEC standard compliant
- 7nm process node
- 410 GB/s maximum bandwidth
- Speed Bins up to 3.2 Gbps
- Support for stacks of 2, 4, 8 or 12 DRAM
Memory Interface Chips
Built for speed, power efficiency and reliability, the DDRn memory interface chips for RDIMM, LRDIMM and NVDIMM server modules deliver top-of-the-line performance and the capacity needed to meet the growing demands on enterprise and data center systems.

**Industry-leading Performance**
- Fully-compliant with the latest JEDEC standards
- Operational speeds up to 3200 Mbps

**Enhanced Margin**
- Wide margin I/O design with advanced programmability
- Exceed JEDEC reliability standards for ESD and EOS

**Optimized Power**
- Advanced power management
- Frequency-based, low-power optimization

**Superior Debug and Serviceability**
- Integrated tools for bring-up and debug
- Works out-of-the-box with no BIOS changes required
Memory Interface Chips

Enabling performance and capacity in server DIMMs

**DDR3 DB & RCD**
- JEDEC Compliant
- Speeds up to 2133 Mbps
- Multiple OEM qualifications

AVAILABLE IN PRODUCTION

**DDR4 DB & RCD**
- JEDEC Compliant
- Speeds up to 3200 Mbps
- Multiple OEM qualifications

AVAILABLE IN PRODUCTION

**NV DDR4 NVRCD**
- JEDEC Compliant
- Speeds up to 3200 Mbps
- Ongoing qualifications

AVAILABLE IN PRODUCTION

**DDR5 DB & RCD**
- Consistent with JEDEC direction

UNDER DEVELOPMENT

Smart tools for easy integration and reduced time to market

LabStation Platform and Buffer BIOS Integration Tool

Validated solutions with partners

SAMSUNG SK hynix Micron
DDR DIMMs Boost Capacity and Bandwidth

DIMM Memory Interface chips reduce the number of loads to enable higher system capacity and performance.

Memory Interface Chips = RCD + DB

DDR5 Registered DIMM (RDIMM)

DDR5 Load Reduced DIMM (LRDIMM)
Thank you