Safe Harbor for Forward-Looking Statements

This presentation contains forward-looking statements regarding our financial prospects, including financial guidance for 3Q-2017, markets, demand for our products, and product development, among other things. Such forward-looking statements are based on current expectations, estimates and projections about the Company’s industry and management’s beliefs and assumptions. These statements are subject to risks and uncertainties which are more fully described in the documents that we file with the SEC, including our 10-Ks, 10-Qs and 8-Ks, and these statements may differ materially from our actual results.

This presentation contains non-GAAP financial measures such as non-GAAP operating Income, margin and EPS, and Adjusted EBITDA and EBITDA margins. We believe the presentation of these non-GAAP measures provide management and investors with meaningful information to understand and analyze our financial performance. Reconciliations of these non-GAAP measures to their most directly comparable GAAP measures can be found in the Appendix to the presentation. However, this presentation should not be considered in isolation or as a substitute for the comparable GAAP measurements, when available.
Data Center

Luc Seraphin
General Manager,
Memory & Interfaces Division
The Data Center
Data • Faster

- **Cores**
  - SerDes PHYs
    - Move data from chip to chip
  - Memory PHYs
    - Move data between chips and memory

- **Chips**
  - Server DIMM Chipsets
    - Enables more capacity at high performance
Building Momentum

Rambus Introduces High Bandwidth Memory PHY on GLOBALFOUNDRIES FX-14™ ASIC Platform using 14nm LPP Process Technology

Rambus Partners with Samsung to Develop 56G SerDes PHY on 10nm LPP Process

Rambus, PLDA and Avery Design Announce Comprehensive PCIe 4.0 Solution

Rambus Launches JEDEC-Standard DDR4 NVRCD for Emerging NVDIMM Applications

GLOBALFOUNDRIES Demonstrates 2.5D High-Bandwidth Memory Solution for Data Center, Networking, and Cloud Applications

Data • Faster • Safer
Real-time Applications Demand More Memory

High-bandwidth memory capacity is critical for real-time applications

- Financial Services: Faster transactions and more accurate assessments
- Health & Life Sciences: Solve complex problems with better, faster results
- Telecom & Cloud: More customer transactions
- Business Intelligence: Better insights and more opportunities
Exponential data growth is driving performance requirements and new architectures. High-speed interconnects are key to data center performance and growth.

Exponential Data Growth Mandates Increased Speed

Source: IDC’s Data Age 2025 Study

Data Created

Size of Global Data Creation

Cloud Services
IoT Devices
Streaming Video
Big Data

Servers
Storage

Wireless Networks
eCommerce
Social Media
The Data Center

Data • Faster

Cores
SerDes PHYs
Move data from chip to chip

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Chips
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Rambus High-speed IP Ecosystem

License IP → SoC → Sell ASIC

ASIC House/ SOC Integrators

Foundry

Design/ Validate IP → Data Center

Networking

Communications

Direct License IP

Technology

Data: Faster: Safer
High-speed Interface IP: The Data Center’s Backbone

Largest data centers require millions of high-speed memory and SerDes cores

- Large Data Centers exceed 100,000 servers
- More than a dozen high-speed interfaces required per server

Exponential growth

- Total data center market expected to double in size between 2015 and 2020*
- Data center cloud usage 30% expected CAGR through 2020*

SoC Cost and Complexity on the Rise

Rising design cost and complexity promotes using proven, high performance margin IP solutions

- In-house design cost increasing
  - Approaching ~200 IP blocks per SoC
  - Over $160M in design implementation costs
  - $10M+ potential revenue loss if late to market due to re-spin

- Low risk solutions ➡ Reduce time-to-market
  - Validated, tested, and silicon proven
  - Qualified with industry Fab partners
  - Robust and high-margin solutions

- More than a PHY vendor
  - History of industry leading memory solutions
  - Integrated customer IP
  - System and packaging design capabilities

Source: SEMICO Research

IP Integration cost based on node, not date
Rambus High-Speed SerDes PHY Solutions

Complete Solutions: SerDes PMA+ PCS, MAC (Partners)

<table>
<thead>
<tr>
<th>Speed</th>
<th>Technology</th>
<th>Standards</th>
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<tbody>
<tr>
<td>16G</td>
<td>28nm &amp; 14nm</td>
<td>PCIe 4/3/2, CEI 11/6, XFI/XAUI, SATA, SAS</td>
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<tr>
<td>28G</td>
<td>14nm &amp; 7nm*</td>
<td>CEI-28/25/11/6, 100/50/25GbE, 10G-KR, FC28, XFI/XAUI</td>
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<td>56G</td>
<td>10nm</td>
<td>CEI-56G MR, CEI-56G LR, CEI-28/25/11, 400GbE, PAM-4/NRZ</td>
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<td>7nm</td>
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</table>

LEAD CUSTOMERS

IN DEVELOPMENT

Integrated tools for easy bring-up and characterization

- **Tx/Rx Component models**
  - Termination, RGC, PLL models, circuit noise sensitivity and transfer, Ro sensitivity, Power supply noise
- **Clocking Architecture**
  - (clock forwarding, strobe, CDR)
- **Channel Models**
  - (Pig, vias, Conn, LC, BP)
- **LinkLab**
- **Eq Architecture models**
  - (Tx, FIR, Linear EQ, DFE, PODE)
- **Eq optimization**
  - (ZPE, MMSE, MinBER w/o Peak power constraint)
- **System Verification Output**
  - Time-domain eye, histogram plots
  - Bit-flip curve, BER contour, statistical eye
  - VT margin @ target BER

Validated solutions with partners

*In Development
# Rambus Memory PHY Solutions

## Memory PHY Solutions for Networking and Data Center

<table>
<thead>
<tr>
<th></th>
<th>DDR4/3</th>
<th>HBM2</th>
<th>HBM3</th>
<th>DDR5</th>
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<tbody>
<tr>
<td>28nm &amp; 14nm</td>
<td>28nm &amp; 14nm</td>
<td>14nm &amp; 7nm*</td>
<td>7nm (4.0)</td>
<td>7nm (5)</td>
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<td><strong>3200Mbps</strong></td>
<td><strong>2000Mbps</strong></td>
<td><strong>Expected 4000Mbps</strong></td>
<td><strong>Expected 4800 – 6400Mbps</strong></td>
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<tr>
<td><strong>x16 – x72-bits</strong></td>
<td><strong>1024-bit</strong></td>
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<td><strong>Complex design architectures</strong></td>
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<td><strong>28nm &amp; 14nm</strong></td>
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<td><strong>HBM3</strong></td>
<td><strong>DDR5</strong></td>
<td></td>
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</tbody>
</table>

### Integrated tools for easy bring-up and characterization

- LabStation Platform
- On-chip Noise Monitor

### Validated solutions with partners

- [Northwest Logic](https://www.northwestlogic.com)
- [ARM](https://www.arm.com)

*In Development*
The Data Center

Data • Faster

Cores
SerDes PHYs
Move data between chips and memory
Memory PHYs
Move data chip and memory

Chips
Server DIMM Chipsets
Enables more capacity at high performance
Extend and Expand Current Technology’s Range

- Server DIMM chipsets continue to expand the potential capacity and performance of DRAM

- Rambus is also continuously exploring alternatives to accelerate the delivery and computation of data to close the latency gap between SCM and storage.
Boost Memory Capacity at Peak Bandwidth

Server DIMM Chipsets enable increased capacity at peak DRAM performance

- Registered DIMM (RDIMM) - RCD
- Load Reduced DIMM (LRDIMM) – RCD + DB
- Load Reduced NVDIMM (LRDIMM) – NVRCD
## Rambus Server DIMM Chipset Solutions

### Server DIMM Chipsets: Delivering performance and capacity

<table>
<thead>
<tr>
<th>Type</th>
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<tr>
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<td>- JEDEC compliant&lt;br&gt;- Speeds up to 2133&lt;br&gt;- Multiple OEM qualifications</td>
</tr>
<tr>
<td>DDR4</td>
<td>- JEDEC compliant&lt;br&gt;- Speeds up to 3200&lt;br&gt;- Multiple OEM qualifications</td>
</tr>
<tr>
<td>DDR4</td>
<td>- JEDEC compliant&lt;br&gt;- Speeds up to 3200&lt;br&gt;- Ongoing qualifications</td>
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<tr>
<td>DDR5</td>
<td>- Consistent with JEDEC direction</td>
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<table>
<thead>
<tr>
<th>Type</th>
<th>Status</th>
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</tr>
<tr>
<td>DDR4</td>
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</tr>
<tr>
<td>DDR4</td>
<td>AVAILABLE IN PRODUCTION</td>
</tr>
<tr>
<td>DDR5</td>
<td>IN DEVELOPMENT</td>
</tr>
</tbody>
</table>

### Smart tools for easy integration and reduced time to market

- [LabStation Platform](#)
- [Buffer Bios Integration Tool](#)

### Validated solutions with partners

- Samsung
- SK hynix
- Micron
Introducing DDR5 Server DIMM Chips

Rambus Announces Industry’s First Functional Silicon of Server DIMM Buffer Chipset Targeted for Next-generation DDR5 Memory Technology

Provides data center architects early path to next-generation memory speeds

SUNNYVALE, Calif. – Sept. 20, 2017 – Rambus Inc. (NASDAQ: RMBS) today announced functional silicon of a double data rate (DDR) server DIMM (dual inline memory module) buffer chip prototype for the next generation DDR5 memory technology. This represents a key milestone for Rambus and the industry’s first silicon-proven memory buffer chip prototype capable of achieving the speeds required for the upcoming DDR5 standard.
Growing Opportunity in Data Center

Source: IHS, Gartner, Semico Research, and Rambus estimates