Memory + Interfaces

Kevin Donnelly
Senior Vice President and General Manager
The World’s Data. Delivered.


- Chips to enable *more* capacity at high-performance for enterprise and data center servers
- Interfaces to deliver data *faster* to chips and memory
- Innovations to make systems with *better* power efficiency, reliability and usability

Digital Universe is massive and growing – projected to double every 2 years

Source: IDC 2014
Big Data Drives Server Growth

Connected Devices

Real-time Applications

Virtualization

Advanced Research

In-memory Databases

Real-time Analytics

Driving demands for faster access to more data with high-speed memory and links
Real-time Applications Demand More Memory

- Financial Services
- Health & Life Sciences
- Telecom & Cloud
- Business Intelligence

Diagram with a CPU at the top, DRAM below it, and icons representing different sectors.
Benefits of Keeping Large Data Sets In Memory

Large performance penalty for insufficient memory capacity due to latency and bandwidth gap between memory and storage
Module buffers are now the bottleneck to achieve memory speed and capacity for all server CPUs using DDR4

Server DIMM Chipset = RCD + DB
The company is announcing plans to sell chips under its own brand for the first time in its 25-year history. The latest move builds on Rambus’s expertise in communications technology associated with memory. Rambus won’t actually manufacture its new chips. Like most semiconductor companies founded since the 1980s, it will hire manufacturing specialists to make them.

Rambus is making an advanced server memory interface chipset, dubbed the RB26 for R+DDR4 memory modules. The chips are like the wheels on Ferraris. They enable memory to keep up with high-speed data processors in enterprise and data center server markets. This new family of chips will enable applications such as data-intensive processing, real-time analytics, virtualization, and in-memory computing with increased speed, reliability, and power efficiency.

Rambus, which started its business 25 years ago as a developer of RDRAM technology, is returning to its roots in memory technology innovation. Seizing the opportunity in a growing market of enterprise servers and datacenters that is screaming for dramatic performance improvements both in bandwidth and capacity, Rambus is rolling out a server memory interface chipset.

DDR4 is really hard to get right at high capacities and high speeds in a reliable way. In a world of Big Data server applications, these high capacities and reliability are paramount, and memory will just keep getting faster in a very technologically-challenging. Quite frankly, server OEMs and ODMs needed a new producer of DDR4 server memory chips, and that new provider is Rambus.
Standard Made Better
RB26 DDR4 Server DIMM Chipset

Industry-leading Performance and Margin
• Compliant with latest JEDEC spec @ 2666 Mbps; built-in support for 2933Mbps
• Wide margin IO design with advanced programmability
• Exceeds JEDEC reliability requirements

Optimized Power
• Frequency-based power optimization

Best-in-class Debug and Serviceability
• Integrated tools for bring-up and debug
• Works out of the box with default system BIOS

Sampling today
Who Needs the Server DIMM Chipset

- Server DRAM capacity expected to more than double in next 3 years
- DDR4 server penetration projected to reach more than 80% in 2017 and 100% in 2019*

*Source: IDC, June 2015
Server DIMM Chipset Roadmap

**Next-Gen Chipsets**

- **RBxx**
  - Performance and margin
  - Optimized power
  - Debug & services
  - Enhanced system performance

- **RBxy**
  - Performance and margin
  - Optimized power
  - Debug & services
  - Enhanced system performance
  - Increased speed
  - Enhanced system reliability

**Technology Considerations:**
- Speeds beyond DDR4
- DRAM scaling limits
- Buffer support for different memory types
- Further power reduction

**RB26**
- Performance and margin @ 2.6Gbps
- Optimized power
- Industry-leading debug & services
R+ Memory Interfaces for Data Center and Mobile

High-performance, low power memory interfaces with improved system margin and flexibility

- **R+ LPDDR3**
  - Supports 2133Mbps, 30% lower power than LPDDR3
  - SoC PHYs compatible with LPDDR4, LPDDR3
- **R+ DDR4**
  - Supports 3200Mbps
  - Designed for high-capacity servers and consumer applications

Partnering for success:
# Rambus Leadership in Memory Solutions

## Interface Type

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<thead>
<tr>
<th>Year Introduced</th>
<th>Max Data Rate</th>
<th>RDRAM</th>
<th>SDRAM</th>
<th>DDR</th>
<th>XDR</th>
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## Features

- Programmable Read Latency
- Variable Block Size
- Core Prefetch
- Dual Edge Clocking
- DLL or PLL on a DRAM
- Advanced Power States
- Programmable Write Delay
- Double Bus Rate Control
- Driver Impedance/On Die Termination Calibration using Precision Resistor
- Fly-By Command/Address
- Timing Deskew/Flexphase
- Bank Grouping/Microthreading
- Channel Equalization Tech.
- Near ground signaling (NGS)
- Multi Channel Die
- On Die Termination of CA signals
- Encoded Data Mask
- Encoded DBI
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Note: This list is not exhaustive. Many of the generically labeled innovations listed in the far left hand column are patented or patent pending. Dates shown refer to when innovations were included in the standard when promulgated (some features may no longer be required to conform to such standard), a commercial product or referenced in a datasheet.
Links are Increasingly Important in Data Centers

- Big Data driving increasing need for high-speed serial links, the backbone of the cloud
- Pervasive across all high-end routers, switches and networking systems
- 100GbE switch ports are growing from current annual run-rate of tens of thousands to handily exceed 10 million by 2019 – Crehan Research

Source: Crehan Research Inc.
R+ Serial Links for Data Centers

High-speed, multi-protocol serial link interfaces optimized for challenging enterprise systems

Demonstrated Excellence
- 15+ years of high-speed SerDes design
- Silicon demonstrated up to 40Gbps(NRZ) SerDes
- Simulation, modeling and design of 56G interfaces, interconnects and systems
- State-of-the-art signal and power integrity internal tool methodology
## Rambus Leadership in High-Speed Signaling

<table>
<thead>
<tr>
<th>Interface Type</th>
<th>Quad Serdes</th>
<th>RaserV SerDes</th>
<th>PCIe 1.0</th>
<th>RaserX SerDes</th>
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<th>PCIe 2.0</th>
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<th>R+ MP SerDes</th>
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<tr>
<td>Max Data Rate</td>
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<td>6.4 Gb/s</td>
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<td>5 Gb/s</td>
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<td>8 Gb/s</td>
<td>10 Gb/s</td>
<td>11.2 Gb/s</td>
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### Features

- **PAM-4 Signaling**
- **Transmitter Pre-Emphasis**
- **Multi-Tap Transmit Equalization**
- **Transmit Compliance Pattern**
- **Adaptive Transmit Equalization**
- **Adaptive Receive Equalization**
- **Partial Response Decision Feedback Equalization**
- **Selectable Tap Decision Feedback**
- **Receiver with Eye Diagram**
- **Receiver with Adaptive Sampling Phase**
- **Fast lock CDR – extra edge samplers**
- **2nd order CDR**

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• Significant opportunities from datacenters growth
• DRAM revenue will grow as we continue to license technology and begin to sell buffer chips to DRAM companies
• SoC revenue will grow as we license our patent portfolio as well as memory and serial link SIP